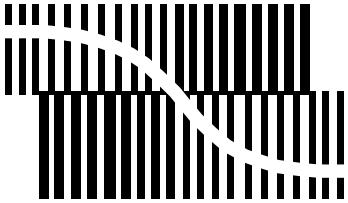
DATA SHEET



UDA1352HL
96 kHz IEC 60958 audio DAC

Preliminary specification

2002 May 22

Philips
Semiconductors

PHILIPS

CONTENTS

1 FEATURES

1.1 General

- 2.4 to 3.6 V power supply
- Integrated digital filter and Digital-to-Analog Converter (DAC)
- $256f_s$ system clock output
- 20-bit data path in interpolator
- High performance
- No analog post filtering required for DAC
- Supporting sampling frequencies from 28 up to 100 kHz.

1.2 Control

- Controlled either by means of static pins, I²C-bus or L3-bus microcontroller interface.

1.3 IEC 60958 input

- On-chip amplifier for converting IEC 60958 input to CMOS levels
- Lock indication signal available on pin LOCK
- Information of the Pulse Code Modulation (PCM) status bit and the non-PCM data detection is available on pin PCMDET
- For left and right 40 key channel-status bits available via L3-bus or I²C-bus interface.

1.4 Digital sound processing and DAC

- Automatic de-emphasis when using IEC 60958 input with 32.0, 44.1 and 48.0 kHz audio sample frequencies
- Soft mute by means of a cosine roll-off circuit selectable via pin MUTE, L3-bus or I²C-bus interface
- Left and right independent dB linear volume control with 0.25 dB steps from 0 to –50 dB, 1 dB steps to –60, –66 and –∞ dB

I²C BUS

BITSTREAM CONVERSION

- Bass boost and treble control in L3-bus or I²C-bus mode
- Interpolating filter (f_s to $64f_s$ or $128f_s$) by means of a cascade of a recursive filter and a FIR filter
- Fifth-order noise shaper (operating either at $64f_s$ or $128f_s$) generates the bitstream for the DAC
- Filter Stream DAC (FSDAC).

2 APPLICATIONS

- Digital audio systems.

3 GENERAL DESCRIPTION

The UDA1352HL is a single-chip IEC 60958 audio decoder with an integrated stereo DAC employing bitstream conversion techniques.

A lock indication signal is available on pin LOCK, indicating that the IEC 60958 decoder is locked. A separate pin PCMDET is available to indicate whether PCM data is applied to the input or not.

By default, the DAC output and the data output interface are muted when the decoder is out-of-lock. However, this setting can be overruled in the L3-bus or I²C-bus mode.

Besides the UDA1352HL, which is the full featured version in LQFP48 package, the UDA1352TS is also available. The UDA1352TS has IEC 60958 input to the DAC only and is in SSOP28 package.

4 ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
UDA1352HL	LQFP48	plastic low profile quad flat package; 48 leads; body 7 × 7 × 1.4 mm	SOT313-2

5 QUICK REFERENCE DATA

V_{DDD} = V_{DDA} = 3.0 V; IEC 60958 input with f_s = 48.0 kHz; T_{amb} = 25 °C; R_L = 5 kΩ; all voltages measured with respect to ground; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
V_{DDD}	digital supply voltage		2.4	3.0	3.6	V
V_{DDA}	analog supply voltage		2.4	3.0	3.6	V
$I_{DDA(DAC)}$	analog supply current of DAC	power-on	–	3.3	–	mA
		power-down; clock off	–	35	–	μA
$I_{DDA(PLL)}$	analog supply current of PLL	at 48 kHz	–	0.5	–	mA
		at 96 kHz	–	0.7	–	mA
$I_{DDD(C)}$	digital supply current of core	at 48 kHz	–	9	–	mA
		at 96 kHz	–	17	–	mA
I_{DDD}	digital supply current	at 48 kHz	–	0.6	–	mA
		at 96 kHz	–	1.2	–	mA
P_{48}	power consumption at 48 kHz	DAC in Playback mode	–	40	–	mW
		DAC in Power-down mode	–	tbf	–	mW
P_{96}	power consumption at 96 kHz	DAC in Playback mode	–	67	–	mW
		DAC in Power-down mode	–	tbf	–	mW
General						
t_{rst}	reset active time		–	250	–	μs
T_{amb}	ambient temperature		–40	–	+85	°C
Digital-to-analog converter						
$V_{o(rms)}$	output voltage (RMS value)	f_i = 1.0 kHz tone at 0 dBFS; note 1	850	900	950	mV
ΔV_o	unbalance of output voltages	f_i = 1.0 kHz tone	–	0.1	0.4	dB
(THD+N)/S	total harmonic distortion-plus-noise to signal ratio	f_i = 1.0 kHz tone at 48 kHz				
		at 0 dBFS	–	–90	–83	dB
		at –40 dBFS; A-weighted	–	–60	–52	dB
		f_i = 1.0 kHz tone at 96 kHz				
		at 0 dBFS	–	–85	–78	dB
		at –40 dBFS; A-weighted	–	–57	–52	dB
S/N_{48}	signal-to-noise ratio at 48 kHz	f_i = 1.0 kHz tone; code = 0; A-weighted	95	100	–	dB
S/N_{96}	signal-to-noise ratio at 96 kHz	f_i = 1.0 kHz tone; code = 0; A-weighted	92	97	–	dB
α_{cs}	channel separation	f_i = 1.0 kHz tone	–	110	–	dB

Note

1. The output voltage of the DAC is proportional to the DAC power supply voltage.

6 BLOCK DIAGRAM

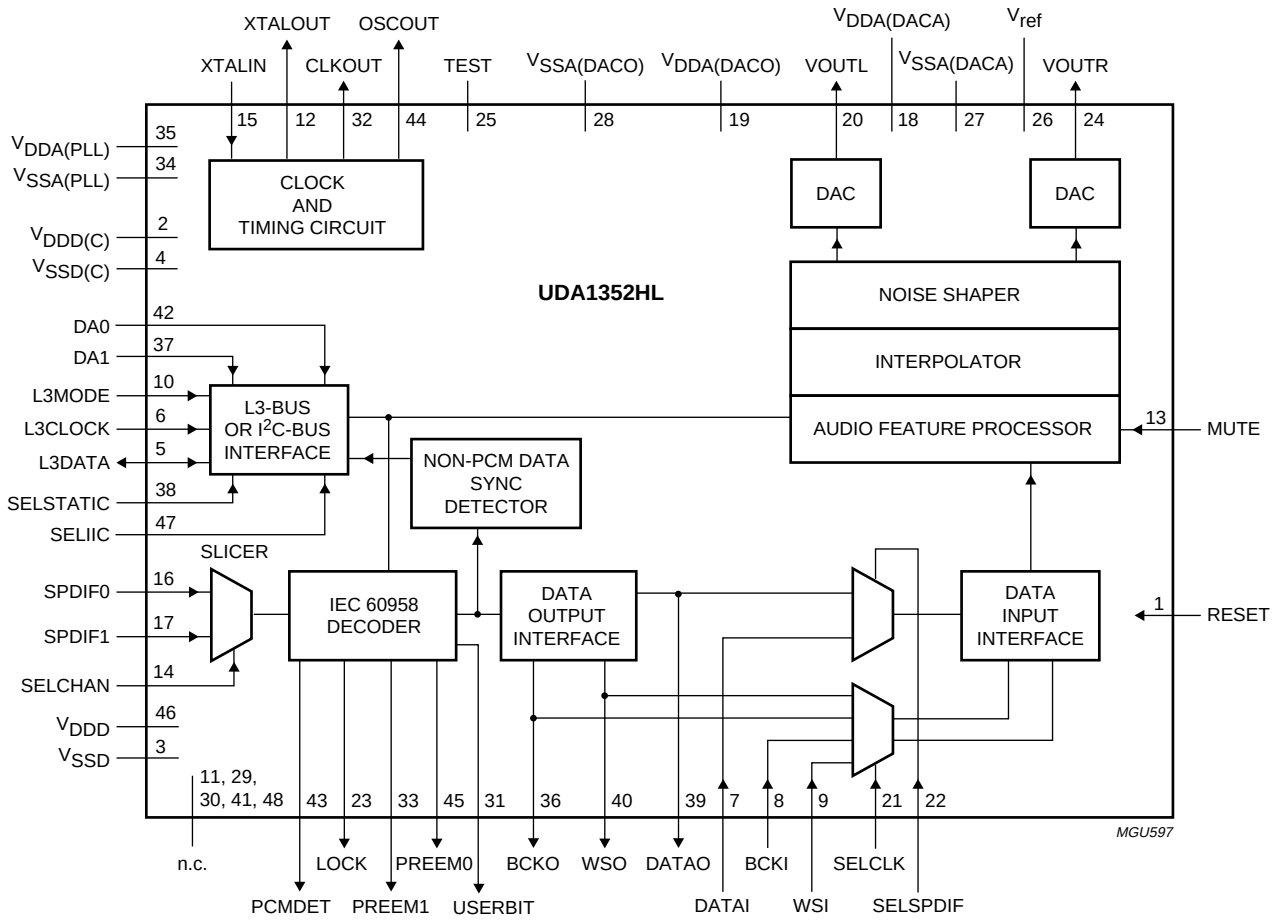


Fig.1 Block diagram.

7 PINNING

SYMBOL	PIN	TYPE[1]	DESCRIPTION
RESET	1	DID	reset input
$V_{DDD(C)}$	2	DS	digital supply voltage for core
V_{SSD}	3	DGND	digital ground
$V_{SSD(C)}$	4	DGND	digital ground for core
L3DATA	5	IIC	L3-bus or I^2C-bus interface data input and output
L3CLOCK	6	DIS	L3-bus or I^2C-bus interface clock input
DATAI	7	DISU	I^2S-bus data input
BCKI	8	DISU	I^2S-bus bit clock input
WSI	9	DISU	I^2S-bus word select input
L3MODE	10	DIS	L3-bus interface mode input
n.c.	11	–	not connected
XTALOUT	12	AIO	crystal oscillator output
MUTE	13	DID	mute control input
SELCHAN	14	DID	IEC 60958 channel selection input
XTALIN	15	AIO	crystal oscillator input
SPDIF0	16	AIO	IEC 60958 channel 0 input
SPDIF1	17	AIO	IEC 60958 channel 1 input
$V_{DDA(DACA)}$	18	AS	analog supply voltage for DAC
$V_{DDA(DACO)}$	19	AS	analog supply voltage for DAC
VOUTL	20	AIO	DAC left channel analog output
SELCLK	21	DID	clock source for PLL selection input
SELSPDIF	22	DIU	IEC 60958 data selection input
LOCK	23	DO	SPDIF and PLL lock indicator output
VOUTR	24	AIO	DAC right channel analog output
TEST	25	DID	test pin; must be connected to digital ground (V_{SSD}) in application
V_{ref}	26	AIO	DAC reference voltage
$V_{SSA(DACA)}$	27	AGND	analog ground for DAC
$V_{SSA(DACO)}$	28	AGND	analog ground for DAC
n.c.	29	–	not connected
n.c.	30	–	not connected
USERBIT	31	DO	user status bit output
CLKOUT	32	DO	clock output ($256f_s$)
PREEM1	33	DO	IEC 60958 input pre-emphasis output 1
$V_{SSA(PLL)}$	34	AGND	analog ground for PLL
$V_{DDA(PLL)}$	35	AS	analog supply voltage for PLL
BCKO	36	DO	I^2S-bus bit clock output
DA1	37	DISU	A1 device address selection input
SELSTATIC	38	DIU	static pin control selection input
DATAO	39	DO	I^2S-bus data output
WSO	40	DO	I^2S-bus word select output

SYMBOL	PIN	TYPE(1)	DESCRIPTION
n.c.	41	–	not connected
DA0	42	DID	A0 device address selection input
PCMDET	43	DO	PCM detection indicator output
OSCOUT	44	DO	internal oscillator output
PREEM0	45	DO	IEC 60958 input pre-emphasis output 0
V_{DDD}	46	DS	digital supply voltage
SELIIC	47	DID	I^2C-bus or L3-bus mode selection input
n.c.	48	–	not connected

Note

1. See Table 1.

Table 1 Pin types

TYPE	DESCRIPTION
DS	digital supply
DGND	digital ground
AS	analog supply
AGND	analog ground
DI	digital input
DIS	digital Schmitt-triggered input
DID	digital input with internal pull-down resistor
DISD	digital Schmitt-triggered input with internal pull-down resistor
DIU	digital input with internal pull-up resistor
DISU	digital Schmitt-triggered input with internal pull-up resistor
DO	digital output
DIO	digital input and output
DIOS	digital Schmitt-triggered input and output
IIC	input and open-drain output for I^2C-bus
AIO	analog input and output

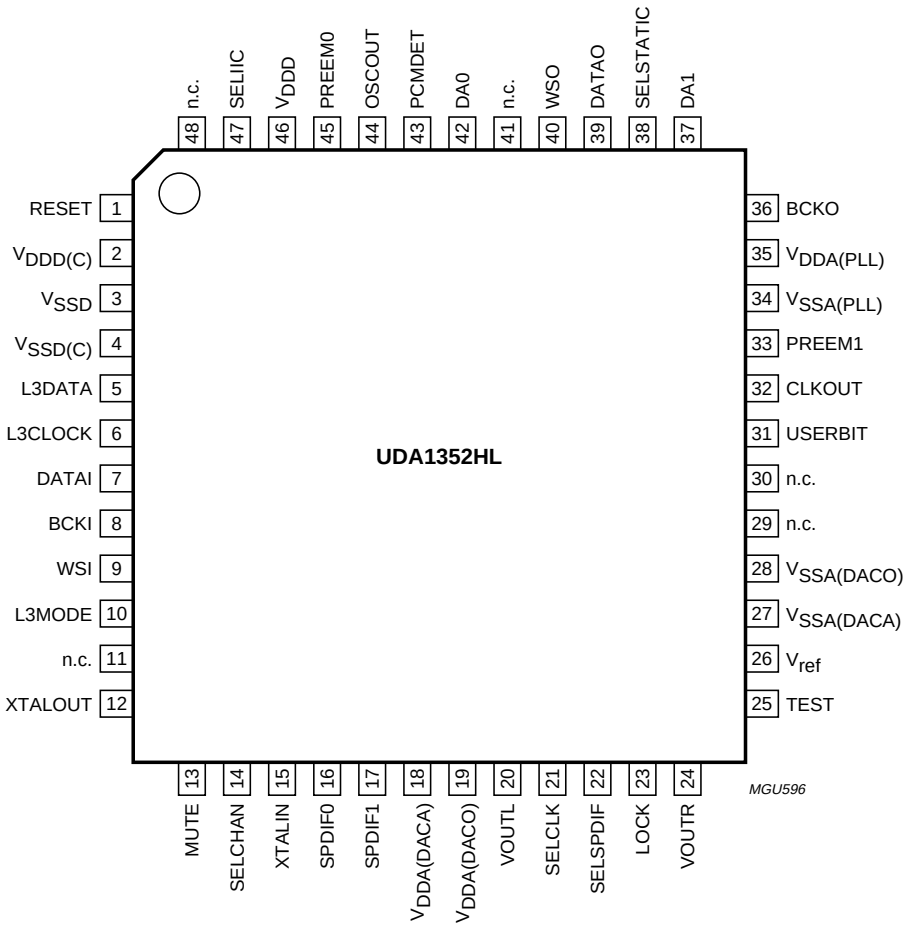


Fig.2 Pin configuration.

8 FUNCTIONAL DESCRIPTION

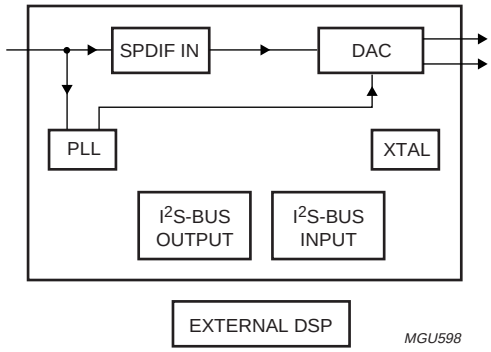
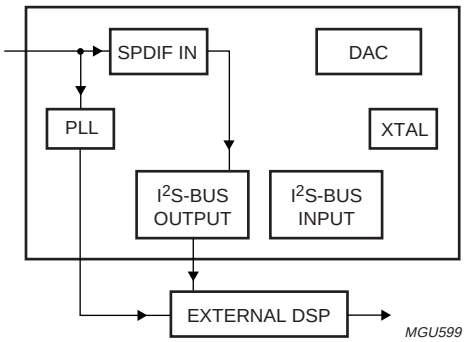
8.1 Operating modes

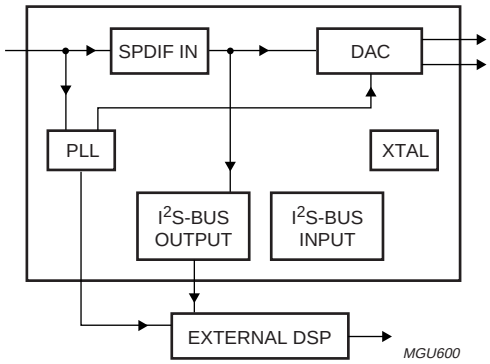
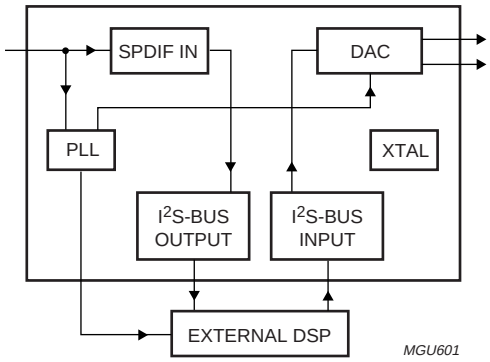
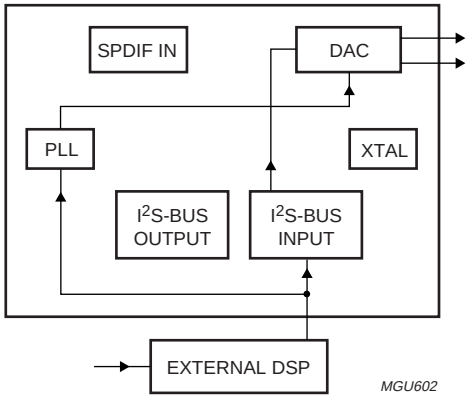
The UDA1352HL is a low cost multi-purpose IEC 60958 decoder DAC with a variety of operating modes.

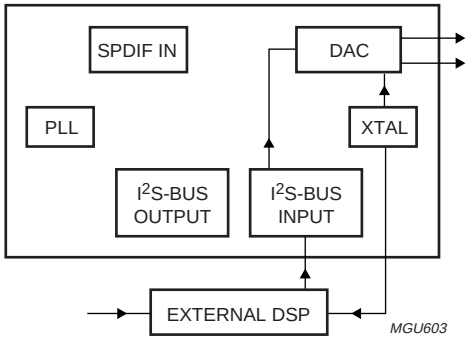
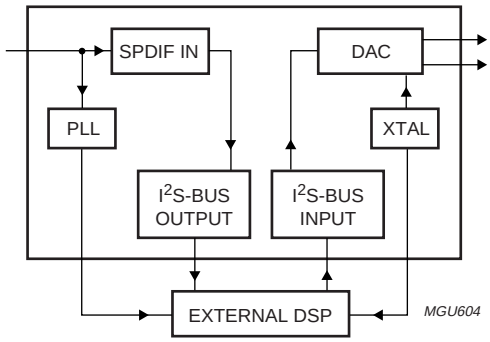
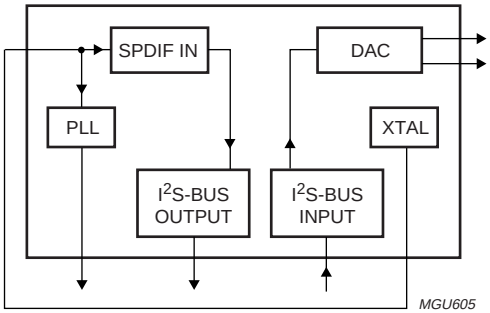
In modes 1, 2, 3, 4, 6, 7 and 8, the UDA1352HL can be clock master; it generates the clock for both the outgoing and incoming digital data streams. Consequently, any device providing data for the UDA1352HL via the data input interface in mode 4 will be slave to the clock generated by the UDA1352HL.

In mode 5 the UDA1352HL locks to signal WSI from the digital data input interface. Conforming to IEC 60958, the audio sample frequency of the data input interface must be between 28.0 and 100.0 kHz.

Mode survey

MODE	FUNCTION	SCHEMATIC
1	IEC 60958 input DAC output The system locks onto the SPDIF signal.	
2	IEC 60958 input I²S-bus digital interface output The system locks onto the SPDIF signal Digital output with BCK and WS is master.	

MODE	FUNCTION	SCHEMATIC
3	IEC 60958 input I²S-bus digital interface output DAC output The system locks onto the SPDIF signal Digital output with BCK and WS is master.	
4	IEC 60958 input I²S-bus digital interface output I²S-bus digital interface input DAC output The system locks onto the SPDIF signal Digital I/O with BCK and WS are master.	
5	I²S-bus digital interface input DAC output The system locks onto the WS signal Digital input with BCK and WS is slave.	

MODE	FUNCTION	SCHEMATIC
6	I^2S-bus digital interface input DAC output The crystal oscillator generates the clocks for system and master clock output Digital input with BCK and WS is master.	
7	IEC 60958 input I^2S-bus digital interface output I^2S-bus digital interface input DAC output SPDIF input to digital interface output is locked onto the SPDIF signal DAC locks onto the crystal oscillator Digital I/O with BCK and WS are master.	
8	Crystal oscillator output for IEC 60958 input I^2S-bus digital interface output The crystal oscillator generates the master clock PLL regenerates the BCK and WS from input clock by setting the pre-scaler ratio Digital output with BCK and WS is master (invalid DATA) Digital input with BCK and WS is slave.	

8.2 Clock regeneration and lock detection

The UDA1352HL contains an on-board PLL for regenerating a system clock from the IEC 60958 input bitstream.

Remark: If there is no input signal, the PLL generates a minimum frequency and the output spectrum shifts accordingly. Since the analog output does not have an analog mute, this means noise that is out of band under normal conditions can move into the audio band.

When the on-board clock locks to the incoming frequency, the lock indicator bit is set and can be read via the L3-bus or I^{2}C-bus interface. Internally, the PLL lock indication can be combined with the PCM status bit of the input data stream and the status whether any burst preamble is detected or not. By default, when both the IEC 60958 decoder and the on-board clock have locked to the incoming signal and the input data stream is PCM data, pin LOCK will be asserted. However, when the IC is locked but the PCM status bit reports non-PCM data, pin LOCK is returned to LOW level. This combination of the lock status and the PCM detection can be overruled by the L3-bus or I^{2}C-bus register setting.

The lock indication output can be used, for example, for muting purposes. The lock signal can be used to drive an external analog muting circuit to prevent out of band noise from becoming audible when the PLL runs at its minimum frequency (e.g. when there is no SPDIF input signal).

The UDA1352HL has a dedicated pin PCMDET to indicate whether valid PCM data stream is detected or (supposed to be) non-PCM data is detected.

8.3 Crystal oscillator

The UDA1352HL has an on-board crystal oscillator. The generated clock can directly operate the DAC as system clock in the modes 6 and 7. Furthermore, it can be obtained from pin OSCOUT. The clock from pin OSCOUT can be applied to the SPDIF inputs.

By setting the UDA1352HL as a frequency synthesizer (mode 8), a wide range of frequency can be obtained. The formula to calculate the system frequency is:

$$f_{sys} = \text{P-ratio} \times f_{OSCOUT} \times \frac{\text{C-ratio}}{768},$$

where:

P-ratio: pre-scaler ratio

f_{OSCOUT}: frequency on pin OSCOUT

C-ratio: coarse ratio.

8.4 Mute

The UDA1352HL is equipped with a cosine roll-off mute in the DSP data path of the DAC part. Muting the DAC (by pin MUTE or via bit MT in the L3-bus or I^{2}C-bus mode), will result in a soft mute, as shown in Fig.3. The cosine roll-off soft mute takes 32×32 samples = 23 ms at 44.1 kHz sampling frequency.

When operating in the L3-bus or I^{2}C-bus mode, the device will mute on start-up. In the L3-bus or I^{2}C-bus mode, it is necessary to explicitly switch off the mute for audio output by means of bit MT in the device register.

In the L3-bus or I^{2}C-bus mode, pin MUTE will at all time mute the output signal. This is in contrast to the UDA1350 and the UDA1351 in which pin MUTE in the L3-bus mode does not have any function.

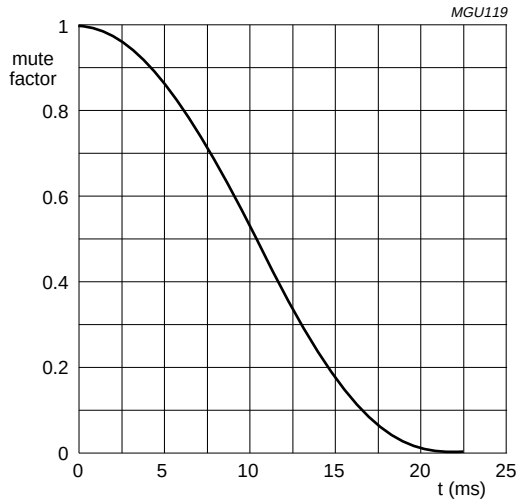


Fig.3 Mute as a function of raised cosine roll-off.

8.5 Auto mute

By default, the DAC outputs will be muted until the UDA1352HL is locked, regardless of the level on pin MUTE or the state of bit MT. In this way, only valid data will be passed to the outputs. This mute is done in the SPDIF interface and is a hard mute, not a cosine roll-off mute.

If needed, this muting can be bypassed by setting bit MUTEBP = 1 via the L3-bus or I^{2}C-bus interface. As a result, the UDA1352HL will no longer mute during out-of-lock situations.

8.6 Data path

The UDA1352HL data path consists of the IEC 60958 decoder, the audio feature processor, the digital interpolator and noise shaper and the DACs.

8.6.1 IEC 60958 INPUT

The IEC 60958 decoder features an on-chip amplifier with hysteresis, which amplifies the SPDIF input signal to CMOS level (see Fig.4).

All 24 bits of data for left and right are extracted from the input bitstream as well as 40 channel status bits for left and right. These bits can be read via the L3-bus or I^{2}C-bus interface.

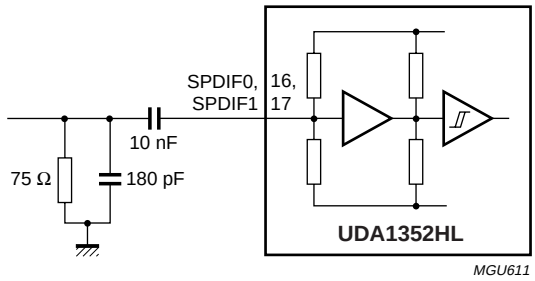


Fig.4 IEC 60958 input circuit and typical application.

The UDA1352HL supports the following sample frequencies and data bit rates:

- f_s = 32.0 kHz, resulting in a data rate of 2.048 Mbits/s
- f_s = 44.1 kHz, resulting in a data rate of 2.8224 Mbits/s
- f_s = 48.0 kHz, resulting in a data rate of 3.072 Mbits/s
- f_s = 64.0 kHz, resulting in a data rate of 4.096 Mbits/s
- f_s = 88.2 kHz, resulting in a data rate of 5.6448 Mbits/s
- f_s = 96.0 kHz, resulting in a data rate of 6.144 Mbits/s.

The UDA1352HL supports timing levels I, II and III, as specified by the IEC 60958 standard. This means that the accuracy of the above mentioned sampling frequencies depends on the timing level I, II or III as mentioned in Section 11.4.1.

8.6.2 AUDIO FEATURE PROCESSOR

The audio feature processor automatically provides de-emphasis for the IEC 60958 data stream in the static pin control mode and default mute at start-up in the L3-bus or I^{2}C-bus mode.

When used in the L3-bus or I^{2}C-bus mode, it provides the following additional features:

- Left and right independent volume control
- Bass boost control
- Treble control
- Mode selection of the sound processing bass boost and treble filters: flat, minimum and maximum
- Soft mute control with raised cosine roll-off
- De-emphasis selection of the incoming data stream for f_s = 32.0, 44.1, 48.0 and 96.0 kHz.

8.6.3 INTERPOLATOR

The UDA1352HL includes an on-board interpolating filter which converts the incoming data stream from $1f_s$ to $64f_s$ or $128f_s$ by cascading a recursive filter and an FIR filter.

Table 2 Interpolator characteristics

PARAMETER	CONDITIONS	VALUE (dB)
Pass-band ripple	0 to $0.45f_s$	±0.03
Stop band	$>0.55f_s$	−50
Dynamic range	0 to $0.45f_s$	114
DC gain	–	−5.67

8.6.4 NOISE SHAPER

The fifth-order noise shaper operates either at $64f_s$ or $128f_s$. It shifts in-band quantization noise to frequencies well above the audio band. This noise shaping technique enables high signal-to-noise ratios to be achieved. The noise shaper output is converted to an analog signal using a filter stream DAC.

8.6.5 FILTER STREAM DAC

The Filter Stream DAC (FSDAC) is a semi-digital reconstruction filter that converts the 1-bit data stream of the noise shaper to an analog output voltage.

The filter coefficients are implemented as current sources and are summed at virtual ground of the output operational amplifier. In this way, very high signal-to-noise performance and low clock jitter sensitivity is achieved. A post filter is not needed due to the inherent filter function of the DAC. On-board amplifiers convert the FSDAC output current to an output voltage signal capable of driving a line output.

The output voltage of the FSDAC is scaled proportionally with the power supply voltage.

8.7 Control

The UDA1352HL can be controlled by means of static pins (when pin SELSTATIC = HIGH), via the I^2C-bus (when pin SELSTATIC = LOW and pin SELIIC = HIGH) or via the L3-bus (when pins SELSTATIC and SELIIC are LOW). For optimum use of the features of the UDA1352HL, the L3-bus or I^2C-bus mode is recommended since only basic functions are available in the static pin control mode.

It should be noted that the static pin control mode and the L3-bus or I^2C-bus mode are mutually exclusive. In the static pin control mode, pins L3MODE and L3DATA are used to select the format for the data output and input interface (see Fig.5).

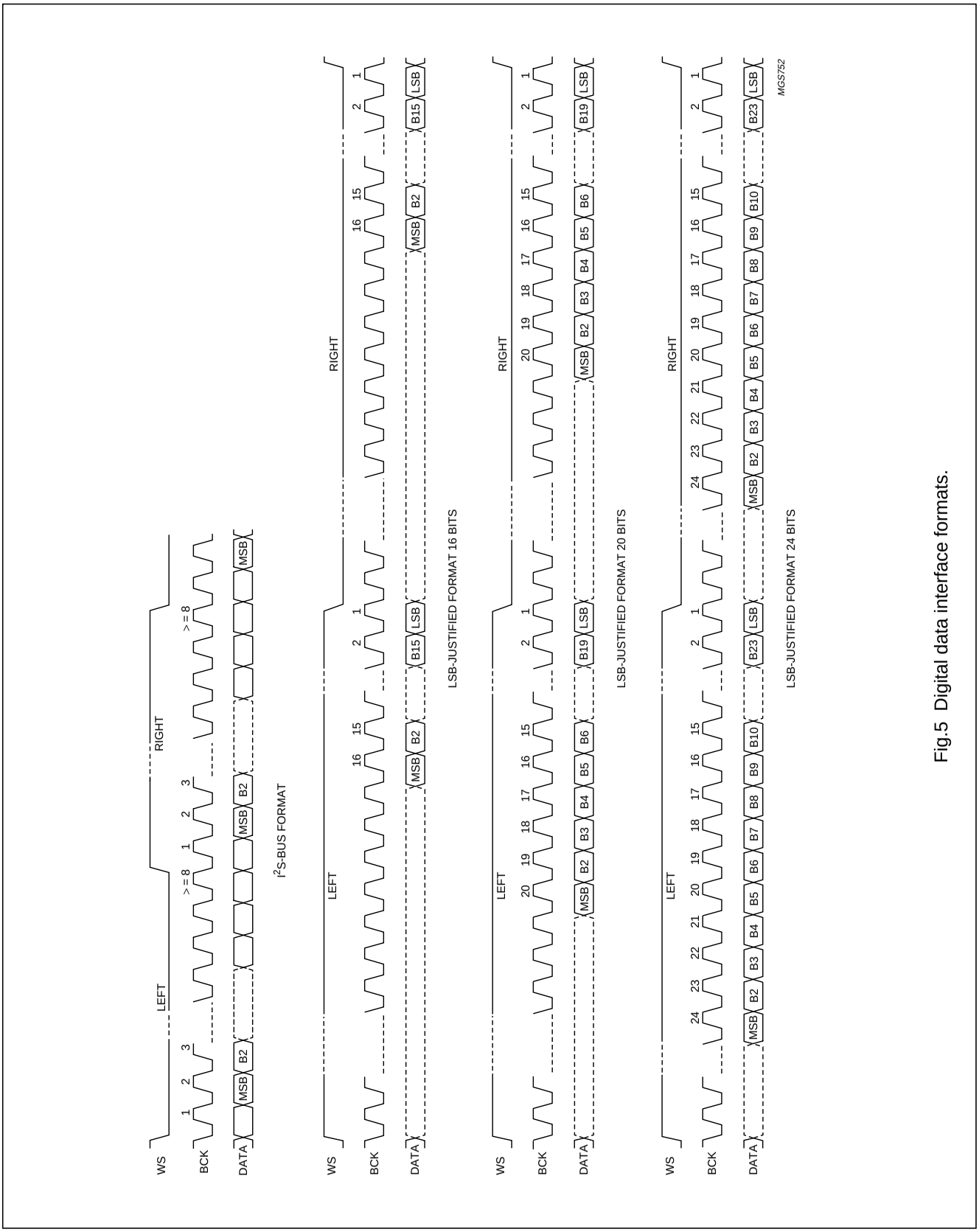


Fig.5 Digital data interface formats.

8.7.1 STATIC PIN CONTROL MODE

The default values for all non-pin controlled settings are identical to the default values at start-up in the L3-bus or I^2C-bus mode (see Table 3).

Table 3 Pin description of static pin control mode

PIN	NAME	VALUE	FUNCTION
Mode selection pin			
38	SELSTATIC	1	select static pin control mode; must be connected to V_{DDD}
Input pins			
1	RESET	0	normal operation
		1	reset
6	L3CLOCK	0	must be connected to V_{SSD}
10 and 5	L3MODE and L3DATA	00	select I^2S-bus format for digital data interface
		01	select LSB-justified format 16 bits for digital data interface
		10	select LSB-justified format 20 bits for digital data interface
		11	select LSB-justified format 24 bits for digital data interface
13	MUTE	0	no mute
		1	mute active
14	SELCHAN	0	select input SPDIF 0 (channel 0)
		1	select input SPDIF 1 (channel 1)
21	SELCLK	0	slave to f_s from IEC 60958; master on data output and input interfaces
		1	slave to f_s from digital data input interface
22	SELSPDIF	0	select data from digital data interface to DAC output
		1	select data from IEC 60958 decoder to DAC output
Status pins			
43	PCMDET	0	non-PCM data or burst preamble detected
		1	PCM data detected
23	LOCK	0	clock regeneration and IEC 60958 decoder out-of-lock or non-PCM data detected
		1	clock regeneration and IEC 60958 decoder locked and PCM data detected
33 and 45	PREEM1 and PREEM0	00	IEC 60958 input; no pre-emphasis
		01	IEC 60958 input; f_s = 32.0 kHz with pre-emphasis
		10	IEC 60958 input; f_s = 44.1 kHz with pre-emphasis
		11	IEC 60958 input; f_s = 48.0 kHz with pre-emphasis
Test pin			
25	TEST	0	must be connected to V_{SSD}

8.7.2 L3-BUS OR I²C-BUS MODE

The L3-bus or I²C-bus mode allows maximum flexibility in controlling the UDA1352HL (see Table 4).

It should be noted that in the L3-bus or I²C-bus mode, several base-line functions are still controlled by pins on the device and that, on start-up in the L3-bus or I²C-bus mode, the output is explicitly muted by bit MT via the L3-bus or I²C-bus interface.

Table 4 Pin description in the L3-bus or I²C-bus mode

PIN	NAME	VALUE	FUNCTION
Mode selection pins			
38	SELSTATIC	0	select L3-bus mode or I²C-bus mode; must be connected to V_{SSD}
47	SELIIC	0	select L3-bus mode; must be connected to V_{SSD}
		1	select I²C-bus mode; must be connected to V_{DDD}
Input pins			
1	RESET	0	normal operation
		1	reset
5	L3DATA	–	must be connected to the L3-bus
		–	must be connected to the SDA line of the I²C-bus
6	L3CLOCK	–	must be connected to the L3-bus
		–	must be connected to the SCL line of the I²C-bus
10	L3MODE	–	must be connected to the L3-bus
13	MUTE	0	no mute
		1	mute active
Status pins			
43	PCMDET	0	non-PCM data or burst preamble detected
		1	PCM data detected
23	LOCK	0	clock regeneration and IEC 60958 decoder out-of-lock or non-PCM data detected
		1	clock regeneration and IEC 60958 decoder locked and PCM data detected
33 and 45	PREEM1 and PREEM0	00	IEC 60958 input; no pre-emphasis
		01	IEC 60958 input; f_s = 32.0 kHz with pre-emphasis
		10	IEC 60958 input; f_s = 44.1 kHz with pre-emphasis
		11	IEC 60958 input; f_s = 48.0 kHz with pre-emphasis
Test pins			
25	TEST	0	must be connected to V_{SSD}

9 L3-BUS DESCRIPTION

9.1 General

The UDA1352HL has an L3-bus microcontroller interface and all the digital sound processing features and various system settings can be controlled by a microcontroller.

The controllable settings are:

- Restoring L3-bus default values
- Power-on
- Selection of filter mode and settings of treble and bass boost
- Volume settings left and right
- Selection of soft mute via cosine roll-off and bypass of auto mute
- Selection of de-emphasis (mode 4 to mode 8 only).

The readable settings are:

- Mute status of interpolator
- PLL locked
- SPDIF input signal locked
- Audio sample frequency
- Valid PCM data detected
- Pre-emphasis of the IEC 60958 input signal
- Accuracy of the clock.

The exchange of data and control information between the microcontroller and the UDA1352HL is LSB first and is accomplished through the serial hardware L3-bus interface comprising the following pins:

- L3DATA: data line
- L3MODE: mode line
- L3CLOCK: clock line.

The L3-bus format has two modes of operation:

- Address mode
- Data transfer mode.

The address mode is used to select a device for a subsequent data transfer. The address mode is characterized by L3MODE being LOW and a burst of 8 pulses on L3CLOCK, accompanied by 8 bits (see Fig.6). The data transfer mode is characterized by L3MODE being HIGH and is used to transfer one or more bytes representing a register address, instruction or data.

Basically, two types of data transfers can be defined:

- Write action: data transfer to the device
- Read action: data transfer from the device.

Remark: when the device is powered-up, at least one L3CLOCK pulse must be given to the L3-bus interface to wake-up the interface before starting sending to the device (see Fig.6). This is only needed once after the device is powered-up.

9.2 Device addressing

The device address consists of 1 byte with:

- Data Operating Mode (DOM) bits 0 and 1 representing the type of data transfer (see Table 5)
- Address bits 2 to 7 representing a 6-bit device address. The bits 2 and 3 of the address can be selected via the external pins DA0 and DA1, which allows up to 4 UDA1352HL devices to be independently controlled in a single application.

The primary address of the UDA1352HL is ‘001000’ (LSB to MSB) and the default address is ‘011000’.

Table 5 Selection of data transfer

DOM		TRANSFER
BIT 0	BIT 1	
0	0	not used
1	0	not used
0	1	write data or prepare read
1	1	read data

9.3 Register addressing

After sending the device address (including DOM bits), indicating whether the information is to be read or written, one data byte is sent using bit 0 to indicate whether the information will be read or written and bits 1 to 7 for the destination register address.

Basically, there are three methods for register addressing:

1. Addressing for write data: bit 0 is logic 0 indicating a write action to the destination register, followed by bits 1 to 7 indicating the register address (see Fig.6)
2. Addressing for prepare read: bit 0 is logic 1, indicating that data will be read from the register (see Fig.7)
3. Addressing for data read action. Here, the device returns a register address prior to sending data from that register. When bit 0 is logic 0, the register address is valid; when bit 0 is logic 1, the register address is invalid.

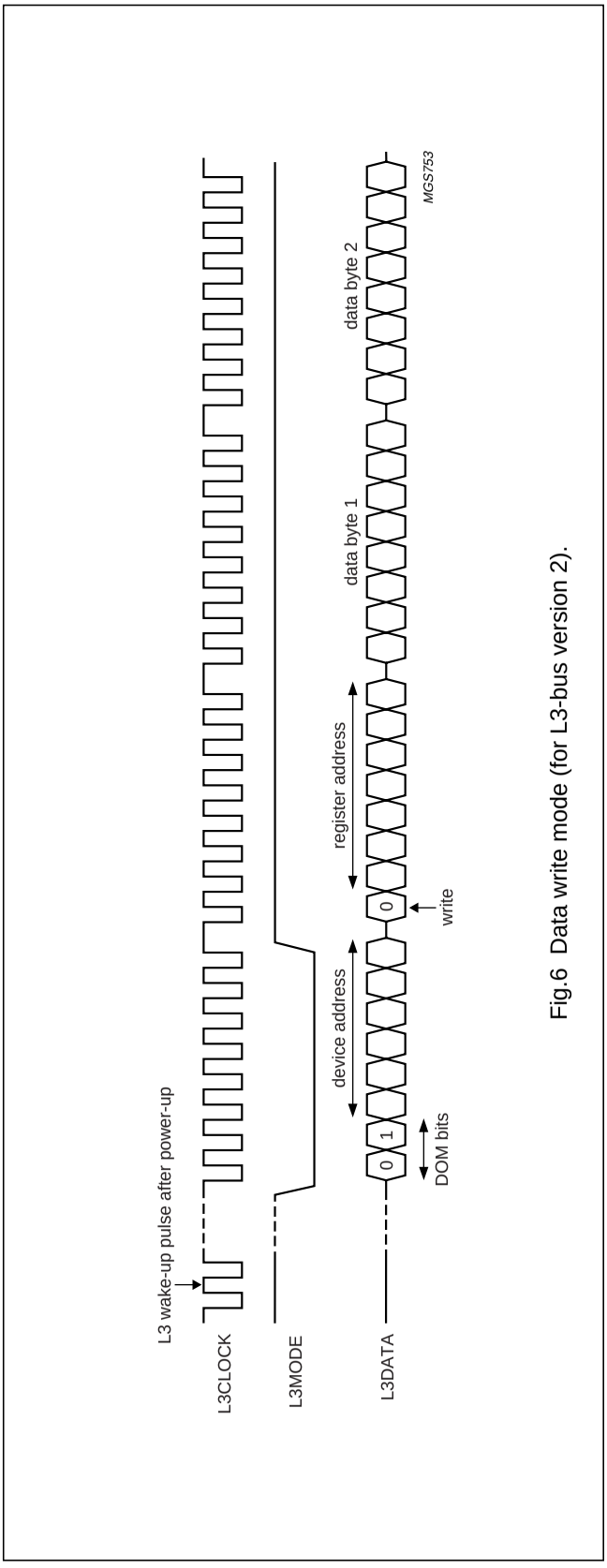


Fig.6 Data write mode (for L3-bus version 2).

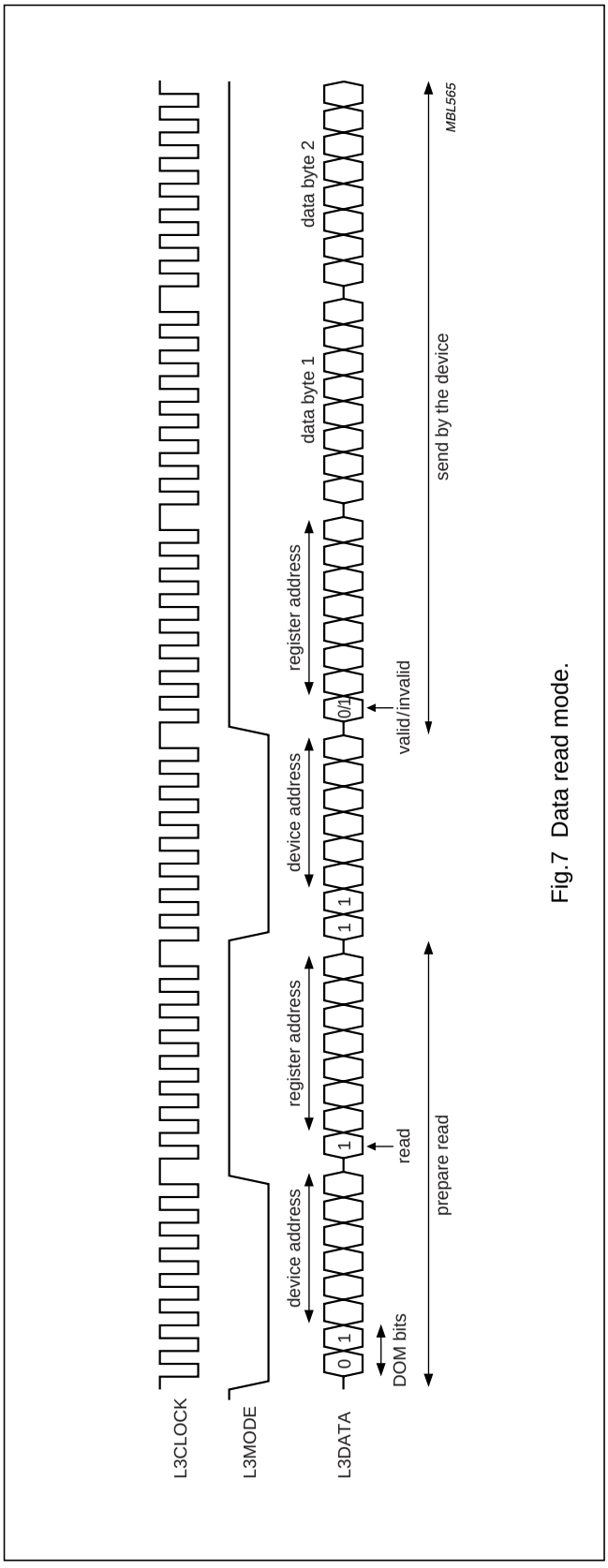


Fig.7 Data read mode.

9.4 Data write mode

The data write mode is explained in the signal diagram of Fig.6. For writing data to a device, 4 bytes must be sent (see Table 6):

1. One byte starting with ‘01’ for signalling the write action to the device, followed by the device address (‘011000’ for the UDA1352HL default)
2. One byte starting with a ‘0’ for signalling the write action, followed by 7 bits indicating the destination register address in binary format with A6 being the MSB and A0 being the LSB
3. One data byte (from the two data bytes) with D15 being the MSB
4. One data byte (from the two data bytes) with D0 being the LSB.

It should be noted that each time a new destination register address needs to be written, the device address must be sent again.

9.5 Data read mode

To read data from the device, a prepare read must first be done and then data read. The data read mode is explained in the signal diagram of Fig.7.

For reading data from a device, the following 6 bytes are involved (see Table 7):

1. One byte with the device address, including ‘01’ for signalling the write action to the device
2. One byte is sent with the register address from which data needs to be read; this byte starts with a ‘1’, which indicates that there will be a read action from the register, followed by seven bits for the source register address in binary format, with A6 being the MSB and A0 being the LSB
3. One byte with the device address preceded by ‘11’ is sent to the device; the ‘11’ indicates that the device must write data to the microcontroller
4. One byte, sent by the device to the bus, with the (requested) register address and a flag bit indicating whether the requested register was valid (bit is logic 0) or invalid (bit is logic 1)
5. One byte (from the two bytes), sent by the device to the bus, with the data information in binary format, with D15 being the MSB
6. One byte (from the two bytes), sent by the device to the bus, with the data information in binary format, with D0 being the LSB.

Table 6 L3-bus write data

BYTE	L3-BUS MODE	ACTION	FIRST IN TIME							LAST IN TIME
			BIT 0	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7
1	address	device address	0	1	DA0	DA1	1	0	0	0
2	data transfer	register address	0	A6	A5	A4	A3	A2	A1	A0
3	data transfer	data byte 1	D15	D14	D13	D12	D11	D10	D9	D8
4	data transfer	data byte 2	D7	D6	D5	D4	D3	D2	D1	D0

Table 7 L3-bus read data

BYTE	L3-BUS MODE	ACTION	FIRST IN TIME							LAST IN TIME
			BIT 0	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7
1	address	device address	0	1	DA0	DA1	1	0	0	0
2	data transfer	register address	1	A6	A5	A4	A3	A2	A1	A0
3	address	device address	1	1	DA0	DA1	1	0	0	0
4	data transfer	register address	0 or 1	A6	A5	A4	A3	A2	A1	A0
5	data transfer	data byte 1	D15	D14	D13	D12	D11	D10	D9	D8
6	data transfer	data byte 2	D7	D6	D5	D4	D3	D2	D1	D0

9.6 Initialization string

For proper and reliable operation, the UDA1352HL must be initialized in the L3-bus mode. This is required for the PLL to start after powering up of the device under all conditions. The initialization string is given in Table 8.

Table 8 L3-bus initialization string and set defaults after power-up

BYTE	L3-BUS MODE	ACTION		FIRST IN TIME							LAST IN TIME
				BIT 0	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7
1	address	init string	device address	0	1	DA0	DA1	1	0	0	0
2	data transfer		register address	0	1	0	0	0	0	0	0
3	data transfer		data byte 1	0	0	0	0	0	0	0	0
4	data transfer		data byte 2	0	0	0	0	0	0	0	1
5	address	set defaults	device address	0	1	DA0	DA1	1	0	0	0
6	data transfer		register address	0	1	1	1	1	1	1	1
7	data transfer		data byte 1	0	0	0	0	0	0	0	0
8	data transfer		data byte 2	0	0	0	0	0	0	0	0

10 I²C-BUS DESCRIPTION

10.1 Characteristics of the I²C-bus

The bus is for 2-way, 2-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to the V_{DD} via a pull-up resistor when connected to the output stages of a microcontroller. For a 400 kHz IC the recommendation for this type of bus from Philips Semiconductors must be followed (e.g. up to loads of 200 pF on the bus a pull-up resistor can be used, between 200 to 400 pF a current source or switched resistor must be used). Data transfer can only be initiated when the bus is not busy.

10.2 Bit transfer

One data bit is transferred during each clock pulse (see Fig.8). The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as control signals. The maximum clock frequency is 400 kHz.

To be able to run on this high frequency all the inputs and outputs connected to this bus must be designed for this high-speed I²C-bus according to specification *"The I²C-bus and how to use it"*, (order code 9398 393 40011).

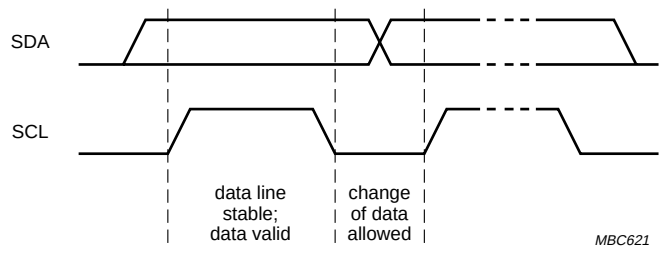


Fig.8 Bit transfer on the I²C-bus.

10.3 Byte transfer

Each byte (8 bits) is transferred with the MSB first (see Table 9).

Table 9 Byte transfer

MSB			BIT NUMBER				LSB
7	6	5	4	3	2	1	0

10.4 Data transfer

A device generating a message is a transmitter, a device receiving a message is the receiver. The device that controls the message is the master and the devices which are controlled by the master are the slaves.

10.5 Start and stop conditions

Both data and clock line will remain HIGH when the bus in not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH, is defined as a start condition (S); see Fig.9. A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as a stop condition (P).

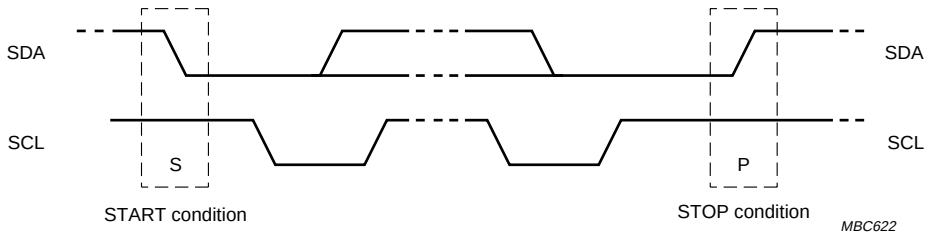


Fig.9 START and STOP conditions on the I^2C-bus.

10.6 Acknowledgment

The number of data bits transferred between the start and stop conditions from the transmitter to receiver is not limited. Each byte of eight bits is followed by one acknowledge bit (see Fig.10). At the acknowledge bit the data line is released by the master and the master generates an extra acknowledge related clock pulse.

A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter.

The device that acknowledges has to pull-down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse. Set-up and hold times must be taken into account. A master receiver must signal an end of data to the transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this event, the transmitter must leave the data line HIGH to enable the master to generate a stop condition.

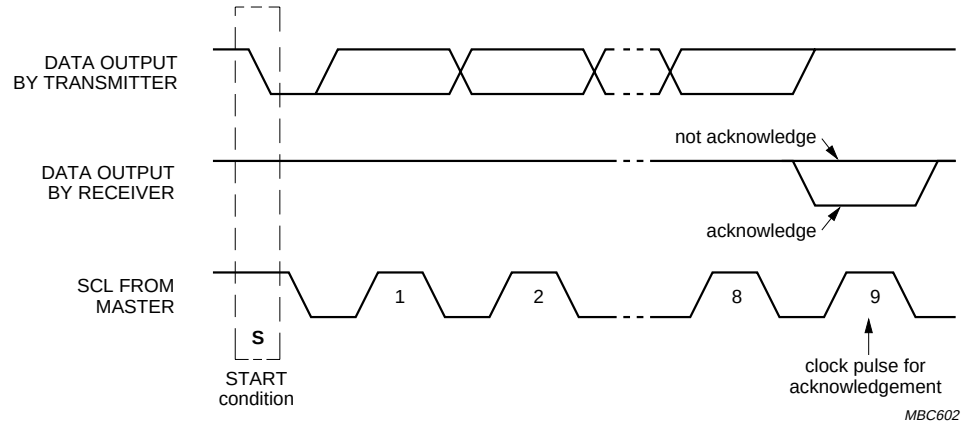


Fig.10 Acknowledge on the I²C-bus.

10.7 Device address

Before any data is transmitted on the I²C-bus, the device which should respond is addressed first. The addressing is always done with byte 1 transmitted after the start procedure.

The device address can be one out of four, being set by pin DA0 and pin DA1.

The UDA1352HL acts as a slave receiver or a slave transmitter. Therefore, the clock signal SCL is only an input signal. The data signal SDA is a bidirectional line. The UDA1352HL device address is shown in Table 10.

Table 10 I²C-bus device address

DEVICE ADDRESS							R/$\overline{W}$
A6	A5	A4	A3	A2	A1	A0	–
1	0	0	1	1	DA1	DA0	0/1

10.8 Register address

The register addresses in the I²C-bus mode are the same as in the L3-bus mode.

10.9 Write and read data

The I²C-bus configuration for a write and read cycle are shown respectively in Tables 11 and 12, respectively. The write cycle is used to write groups of two bytes to the internal registers for the digital sound feature control and system setting. It is also possible to read these locations for the device status information.

10.10 Write cycle

The I²C-bus configuration for a write cycle is shown in Table 11. The write cycle is used to write the data to the internal registers. The device and register addresses are one byte each, the setting data is always a pair of two bytes.

The format of the write cycle is as follows:

1. The microcontroller starts with a start condition (S).
2. The first byte (8 bits) contains the device address ‘1001 110’ and a logic 0 (write) for the R/$\overline{W}$ bit.
3. This is followed by an acknowledge (A) from the UDA1352HL.
4. After this the microcontroller writes the 8-bit register address (ADDR) where the writing of the register content of the UDA1352HL must start.
5. The UDA1352HL acknowledges this register address (A).
6. The microcontroller sends 2 bytes data with the Most Significant (MS) byte first and then the Least Significant (LS) byte. After each byte an acknowledge is followed from the UDA1352HL.
7. If repeated groups of 2 bytes are transmitted, then the register address is auto incremented. After each byte an acknowledge is followed from the UDA1352HL.
8. Finally, the UDA1352HL frees the I²C-bus and the microcontroller can generate a stop condition (P).

Table 11 Master transmitter writes to the UDA1352HL registers in the I²C-bus mode.

	DEVICE ADDRESS	**R/$\overline{W}$**		**REGISTER ADDRESS**		**DATA 1**				**DATA 2**(1)				**DATA n**(1)				
S	1001 110	0	A	ADDR	A	MS1	A	LS1	A	MS2	A	LS2	A	MSn	A	LSn	A	P
	acknowledge from UDA1352HL																	

Note

1. Auto increment of register address.

10.11 Read cycle

The read cycle is used to read the data values from the internal registers. The I²C-bus configuration for a read cycle is shown in Table 12.

The format of the read cycle is as follows:

1. The microcontroller starts with a start condition (S).
2. The first byte (8 bits) contains the device address ‘1001 110’ and a logic 0 (write) for the R/$\overline{W}$ bit.
3. This is followed by an acknowledge (A) from the UDA1352HL.
4. After this the microcontroller writes the register address (ADDR) where the reading of the register content of the UDA1352HL must start.
5. The UDA1352HL acknowledges this register address.
6. Then the microcontroller generates a repeated start (Sr).
7. Then the microcontroller generates the device address ‘1001 110’ again, but this time followed by a logic 1 (read) of the R/$\overline{W}$ bit. An acknowledge is followed from the UDA1352HL.
8. The UDA1352HL sends 2 bytes data with the Most Significant (MS) byte first and then the Least Significant (LS) byte. After each byte an acknowledge is followed from the microcontroller.
9. If repeated groups of 2 bytes are transmitted, then the register address is auto incremented. After each byte an acknowledge is followed from the microcontroller.
10. The microcontroller stops this cycle by generating a negative acknowledge (NA).
11. Finally, the UDA1352HL frees the I²C-bus and the microcontroller can generate a stop condition (P).

Table 12 Master transmitter reads from the UDA1352HL registers in the I²C-bus mode.

	DEVICE ADDRESS	**R/$\overline{W}$**		**REGISTER ADDRESS**			**DEVICE ADDRESS**	**R/$\overline{W}$**		**DATA 1**				**DATA 2**(1)				**DATA n**(1)				
S	1001 110	0	A	ADDR	A	Sr	1001 110	1	A	MS1	A	LS1	A	MS2	A	LS2	A	MSn	A	LSn	NA	P
	acknowledge from UDA1352HL									acknowledge from master												

Note

1. Auto increment of register address.

11 SPDIF SIGNAL FORMAT

11.1 SPDIF channel encoding

The digital signal is coded using Bi-phase Mark Code (BMC), which is a kind of phase-modulation. In this scheme, a logic one in the data corresponds to two zero-crossings in the coded signal, and a logic zero to one zero-crossing. An example of the encoding is given in Fig.11.

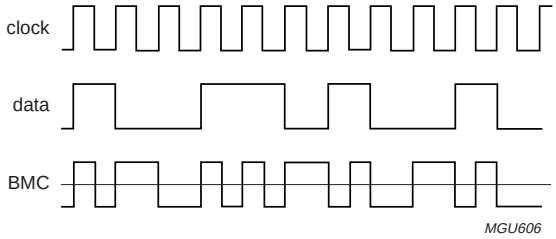


Fig.11 Bi-phase mark encoding.

11.2 SPDIF hierarchical layers for audio data

From an abstract point of view an SPDIF signal can be represented as in Fig.12. A 2 channel PCM signal can be transmitted as various sequential blocks. Each block in turn consists of 192 frames. Each frame contains two sub-frames, one for each channel.

Each sub-frame is preceded by a preamble. There are three types of preambles being B, M and W. Preambles can be spotted easily in an SPDIF stream because these sequences can never occur in the channel parts of a valid SPDIF stream. Table 13 indicates the values of the preambles.

A sub-frame in turn contains a single audio sample which may be up to 24 bits wide, a validity bit which indicates whether the sample is valid, a single bit of user data, and a single bit of channel status. Finally there is a parity bit for this particular sub-frame (see Fig.13).

The data bits from 4 to 31 in each sub-frame will be modulated using a BMC scheme. The sync preamble actually contains a violation of the BMC scheme and consequently can be detected easily.

Table 13 Preambles

PRECEDING STATE	CHANNEL CODING	
	0	1
B	1110 1000	0001 0111
M	1110 0010	0001 1101
W	1110 0100	0001 1011

11.3 SPDIF hierarchical layers for digital data

The difference with the audio format is that the data contained in the SPDIF signal is not audio but is digital data.

When transmitting digital data via SPDIF using the IEC 60958 protocol, the allocation of the bits inside the data word is done as shown in Table 14.

Table 14 Bit allocation for digital data

FIELD	IEC 60958 TIME SLOT BITS	DESCRIPTION
0 to 3	preamble	IEC 60958 preamble
4 to 7	auxiliary bits	not used; all logic 0
8 to 11	unused data bits	not used; all logic 0
12	16 bits data	sections of the digital bitstream
13	user data	according to IEC 60958
14 to 27	16 bits data	sections of the digital bitstream
28	validity bit	according to IEC 60958
29	user bit	according to IEC 60958
30	channel status bit	according to IEC 60958
31	parity bit	according to IEC 60958

As shown in Table 14 and Fig.14, the non-PCM encoded data bitstreams are transferred within the basic 16 bits data area of the IEC 60958 sub-frames [time-slots 12 (LSB) to 27 (MSB)].

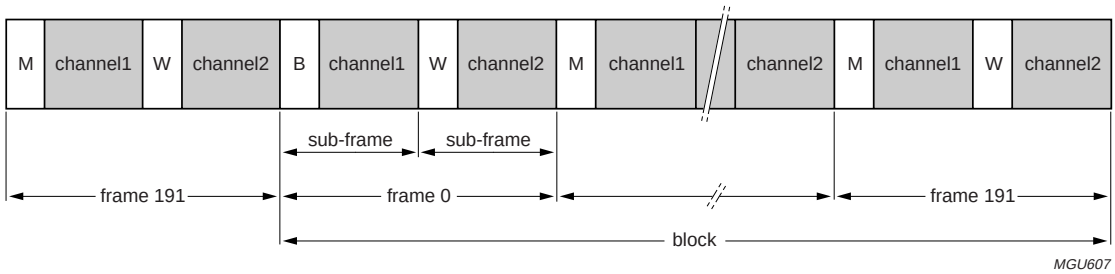


Fig.12 SPDIF block format.

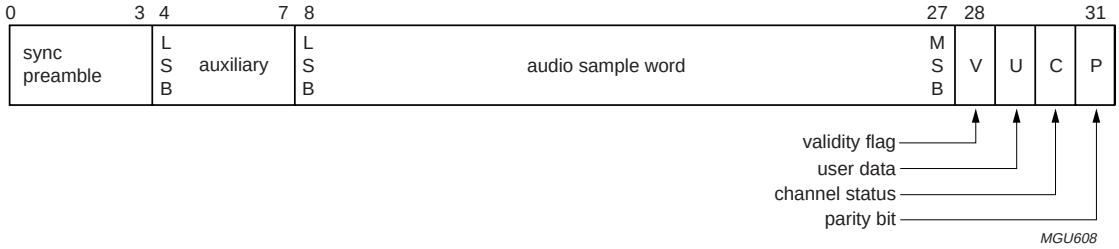


Fig.13 Sub-frame format in audio mode.

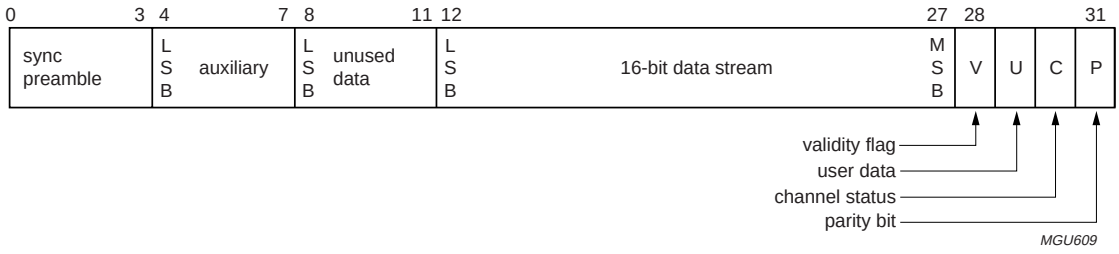


Fig.14 Sub-frame format in non-PCM mode.

11.3.1 Format of the bitstream

The non-PCM data is transmitted in data bursts, consisting of four 16-bit words (called Pa, Pb, Pc and Pd) followed by the so called burst-payload. The definition of the burst preambles is given in Table 15.

Table 15 Burst preamble words

PREAMBLE WORD	LENGTH OF THE FIELD	CONTENTS	VALUE
Pa	16 bits	sync word 1	F872 (hex)
Pb	16 bits	sync word 2	4E1F (hex)
Pc	16 bits	burst information	see Table 16
Pd	16 bits	length code	number of bits

11.3.2 Burst information

The burst information given in preamble Pc, meaning the information contained in the data stream, is defined according to IEC 60958 as given in Table 16.

Table 16 Fields of burst information in preamble Pc

BITS OF Pc	VALUE	CONTENTS	REFERENCE POINT R	REPETITION TIME OF DATA BURST IN IEC 60958 FRAMES
0 to 4	0	NULL data	–	none
	1	AC-3 data	R_AC-3	1536
	2	reserved	–	–
	3	pause	bit 0 of Pa	refer to IEC 60958
	4	MPEG-1 layer 1 data	bit 0 of Pa	384
	5	MPEG-1 layer 1, 2 or 3 data or MPEG-2 without extension	bit 0 of Pa	1152
	6	MPEG-2 with extension	bit 0 of Pa	1152
	7	reserved	–	–
	8	MPEG-2, layer 1 low sampling rate	bit 0 of Pa	768
	9	MPEG-2, layer 2 or 3 low sampling rate	bit 0 of Pa	2304
	10	reserved	–	–
	11 to 13	reserved (DTS)	–	refer to IEC 61937
	14 to 31	reserved	–	–
5 to 6	0	reserved	–	–
7	0	error flag indicating a valid burst-payload	–	–
	1	error flag indicating an invalid burst-payload	–	–
8 to 12	–	data type dependant info	–	–
13 to 15	0	bitstream number	–	–

11.3.3 Minimum burst spacing

In order to be able to detect the start of a data burst, it is prescribed to have a data-burst which does not exceed 4096 frames. After 4096 frames there must be a synchronisation sequence containing 2 frames of complete zero data (being 4 times 16 bits) followed by the preamble burst Pa and Pb. This way a comparison with a sync code of 96 bits can detect the start of a new burst-payload including the Pc and Pd preambles containing additional stream information.

11.3.4 User bit

The UDA1352HL provides pin USERBIT to read out user data bitstream.

The USERBIT output is synchronized with the WSO output (see Fig.15).

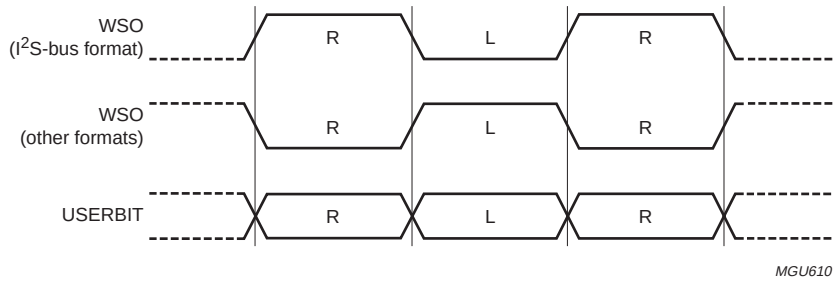


Fig.15 USERBIT output timing.

11.4 Timing characteristics

11.4.1 Frequency requirements

The SPDIF specification IEC 60958 supports three levels of clock accuracy, being:

- Level I, high accuracy: Tolerance of transmitting sampling frequency shall be within 50×10^{-6}
- Level II, normal accuracy: All receivers should receive a signal of 1000×10^{-6} of nominal sampling frequency
- Level III, variable pitch shifted clock mode: A deviation of 12.5% of the nominal sampling frequency is possible.

11.4.2 Rise and fall times

Rise and fall times (see Fig.16) are defined as:

$$\text{Rise time} = \frac{t_r}{(t_L + t_H)} \times 100\%$$

$$\text{Fall time} = \frac{t_f}{(t_L + t_H)} \times 100\%$$

Rise and fall times should be in the range:

- 0% to 20% when the data bit is a logic 1
- 0% to 10% when the data bits are two succeeding logic zeros.

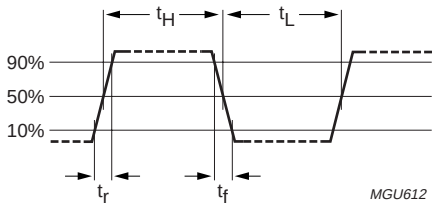


Fig.16 Rise and fall times.

11.4.3 Duty cycle

The duty cycle (see Fig.16) is defined as:

$$\text{Duty cycle} = \frac{t_H}{(t_L + t_H)} \times 100\%$$

The duty cycle should be in the range:

- 40% to 60% when the data bit is a logic 1
- 45% to 55% when the data bits are two succeeding logic zeros.

12 REGISTER MAPPING

Table 17 Register map of control settings (write)

REGISTER ADDRESS	FUNCTION
System settings	
00H	clock settings
01H	I^2S-bus output settings
02H	I^2S-bus input settings
03H	power-down settings
Interpolator	
10H	volume control left and right
12H	sound feature mode, treble and bass boost
13H	de-emphasis and mute
14H	DAC source and clock settings
SPDIF input settings	
30H	SPDIF input settings
Supplemental settings	
40H	supplemental settings
FPLL settings	
62H	FPLL coarse ratio
Software reset	
7FH	restore L3-bus default values

Table 18 Register map of status bits (read-out)

REGISTER ADDRESS	FUNCTION
Interpolator	
18H	interpolator status
SPDIF input	
59H	SPDIF status
5AH	channel status bits left [15:0]
5BH	channel status bits left [31:16]
5CH	channel status bits left [39:32]
5DH	channel status bits right [15:0]
5EH	channel status bits right [31:16]
5FH	channel status bits right [39:32]
FPLL	
68H	FPLL status
Device information	
7EH	device information

12.1 Clock settings (write)

Table 19 Register address 00H

BIT	15	14	13	12	11	10	9	8
Symbol	–	–	–	–	POSTDIV1	POSTDIV0	XTAL_DIV1	XTAL_DIV0
Default	–	–	–	–	0	0	0	0

BIT	7	6	5	4	3	2	1	0
Symbol	FREQ_ SYNTH1	–	–	XRATIO2	XRATIO1	XRATIO0	CLKOUT_ SEL	FREQ_ SYNTH0
Default	0	–	–	0	0	0	0	0

Table 20 Description of register bits

BIT	SYMBOL	DESCRIPTION
15 to 12	–	reserved
11 to 10	POSTDIV[1:0]	reserved
9 to 8	XTAL_DIV[1:0]	**Clock divider settings.** A 2-bit value to set the ratio between the crystal frequency and the DAC sampling frequency in crystal operation mode (DAC clock is $64f_s$). Default value 00, see Table 21.
7	FREQ_SYNTH1	**Frequency synthesizer source setting.** A 1-bit value to set the clock source of the frequency synthesizer. If this bit is logic 0, the SPDIF inputs are used. If this bit is logic 1, then the crystal oscillator output is selected internally. Default value 0.
6 to 5	–	reserved
4 to 2	XRATIO[2:0]	**Pre-scaler ratio settings.** A 3-bit value to set the pre-scaler ratio when the frequency synthesizer is enabled (FREQ_SYNTH0 is logic 1). Default value 000, see Table 22.
1	CLKOUT_SEL	**Clock output select.** A 1-bit value to select the clock signal to be output on pin CLKOUT. If this bit is logic 0, then the clock signal is recovered from the SPDIF or WSI input signal. If this bit is logic 1, then the clock signal comes from the crystal oscillator. Default value 0.
0	FREQ_SYNTH0	**Frequency synthesizer mode.** A 1-bit value to enable the frequency synthesizer mode. If this bit is logic 0, then the frequency synthesizer mode is disabled. If this bit is logic 1, then the frequency synthesizer mode is enabled. Default value 0.

Table 21 Crystal divider settings

XTAL_DIV1	XTAL_DIV0	CRYSTAL CLOCK AND RATIO
0	0	$128f_s$; ratio 1:2 (default)
0	1	$256f_s$; ratio 1:4
1	0	$384f_s$; ratio 1:6
1	1	$512f_s$; ratio 1:8

Table 22 Pre-scaler ratio settings

XRATIO2	XRATIO1	XRATIO0	PRE-SCALER RATIO
0	0	0	1:36 (default)
0	0	1	1:625
0	1	0	1:640
0	1	1	1:1125
1	0	0	reserved
1	0	1	reserved
1	1	0	reserved
1	1	1	reserved

12.2 I²S-bus output settings (write)

Table 23 Register address 01H

BIT	15	14	13	12	11	10	9	8
Symbol	–	–	–	–	–	–	–	MUTEBP
Default	–	–	–	–	–	–	–	0

BIT	7	6	5	4	3	2	1	0
Symbol	BCKWSOUT_DIS	–	–	–	–	SFORO2	SFORO1	SFORO0
Default	0	–	–	–	–	0	0	0

Table 24 Description of register bits

BIT	SYMBOL	DESCRIPTION
15 to 9	–	reserved
8	MUTEBP	**Mute bypass setting.** A 1-bit value to disable the mute bypass setting. When this mute bypass setting is enabled, then even in out-of-lock situations or non-PCM data detected, the output data will not be suppressed. If this bit is logic 0, then the output will be muted in out-of-lock situations. If this bit is logic 1, then the output will not be muted in out-of-lock situations. Default value 0.
7	BCKWSOUT_DIS	**BCKO and WSO output control.** A 1-bit value to disable the WSO and BCKO outputs while the FPLL or SPDIF decoder is out-of-lock. If this bit is logic 0, then the WSO and BCKO outputs are enabled regardless of whether in-lock or out-of-lock. If this bit is logic 1, then the outputs are fixed to logic 0 while the FPLL or SPDIF decoder is out-of-lock. Default value 0.
6 to 3	–	reserved
2 to 0	SFORO[2:0]	**Digital data output formats.** A 3-bit value to set the digital output format. Default value 000, see Table 25.

Table 25 Digital data output formats

SFORO2	SFORO1	SFORO0	FORMAT
0	0	0	I²S-bus (default)
0	0	1	LSB-justified, 16 bits
0	1	0	LSB-justified, 18 bits
0	1	1	LSB-justified, 20 bits
1	0	0	LSB-justified, 24 bits
1	0	1	MSB-justified
1	1	0	reserved
1	1	1	

12.3 I²S-bus input settings (write)

Table 26 Register address 02H

BIT	15	14	13	12	11	10	9	8
Symbol	–	–	–	–	–	–	–	–
Default	–	–	–	–	–	–	–	–

BIT	7	6	5	4	3	2	1	0
Symbol	–	–	–	–	–	SFORI2	SFORI1	SFORI0
Default	–	–	–	–	–	0	0	0

Table 27 Description of register bits

BIT	SYMBOL	DESCRIPTION
15 to 3	–	reserved
2 to 0	SFORI[2:0]	**Digital data input formats.** A 3-bit value to set the digital input format. Default value 000, see Table 28.

Table 28 Digital data input formats

SFORI2	SFORI1	SFORI0	FORMAT
0	0	0	I²S-bus (default)
0	0	1	LSB-justified, 16 bits
0	1	0	LSB-justified, 18 bits
0	1	1	LSB-justified, 20 bits
1	0	0	LSB-justified, 24 bits
1	0	1	MSB-justified
1	1	0	reserved
1	1	1	

12.4 Power-down settings (write)

Table 29 Register address 03H

BIT	15	14	13	12	11	10	9	8
Symbol	–	–	PONVCO	PON_XTAL	–	–	–	–
Default	–	–	1	0	–	–	–	–

BIT	7	6	5	4	3	2	1	0
Symbol	–	–	–	PON_ SPDIFIN	–	–	EN_INT	PONDAC
Default	–	–	–	1	–	–	1	1

Table 30 Description of register bits

BIT	SYMBOL	DESCRIPTION
15 to 14	–	reserved
13	PONVCO	**Power control VCO.** A 1-bit value to switch the VCO into power-on or power-down mode. If this bit is logic 0, then the VCO is in power-down mode. If this bit is logic 1, then the VCO is in power-on mode. Default value 1.
12	PON_XTAL	**Crystal oscillator operation.** A 1-bit value to control the crystal oscillator operation. If this bit is logic 0, then the crystal oscillator is turned off. If this bit is logic 1, then the crystal oscillator is turned on. Default value 0.
11 to 5	–	reserved
4	PON_SPDIFIN	**Power control SPDIF input.** A 1-bit value to enable or disable the power of the IEC 60958 bit slicer. If this bit is logic 0, then the power is off. If this bit is logic 1, then the power is on. Default value 1.
3 to 2	–	reserved
1	EN_INT	**Interpolator clock control.** A 1-bit value to control the interpolator clock. If this bit is logic 0, then the interpolator clock is disabled. If this bit is logic 1, then the interpolator clock is enabled. Default value 1.
0	PONDAC	**Power control DAC.** A 1-bit value to switch the DAC into power-on or power-down mode. If this bit is logic 0, then the DAC is in power-down mode. If this bit is logic 1, then the DAC is in power-on mode. Default value 1.

12.5 Volume control left and right (write)

Table 31 Register address 10H

BIT	15	14	13	12	11	10	9	8
Symbol	VCL_7	VCL_6	VCL_5	VCL_4	VCL_3	VCL_2	VCL_1	VCL_0
Default	0	0	0	0	0	0	0	0

BIT	7	6	5	4	3	2	1	0
Symbol	VCR_7	VCR_6	VCR_5	VCR_4	VCR_3	VCR_2	VCR_1	VCR_0
Default	0	0	0	0	0	0	0	0

Table 32 Description of register bits

BIT	SYMBOL	DESCRIPTION
15 to 8	VCL_[7:0]	**Volume setting left channel.** A 8-bit value to program the left channel volume attenuation. The range is 0 to –50 dB in steps of 0.25 dB, to –60 dB in steps of 1 dB, –66 dB and –∞ dB. Default value 0000 0000, see Table 33.
7 to 0	VCR_[7:0]	**Volume setting right channel.** A 8-bit value to program the right channel volume attenuation. The range is 0 to –50 dB in steps of 0.25 dB, to –60 dB in steps of 1 dB, –66 dB and –∞ dB. Default value 0000 0000, see Table 33.

Table 33 Volume settings left and right channel

VCL_7	VCL_6	VCL_5	VCL_4	VCL_3	VCL_2	VCL_1	VCL_0	VOLUME (dB)
VCR_7	VCR_6	VCR_5	VCR_4	VCR_3	VCR_2	VCR_1	VCR_0	
0	0	0	0	0	0	0	0	0 (default)
0	0	0	0	0	0	0	1	–0.25
0	0	0	0	0	0	1	0	–0.5
:	:	:	:	:	:	:	:	:
1	1	0	0	0	1	1	1	–49.75
1	1	0	0	1	0	0	0	–50
1	1	0	0	1	1	0	0	–51
1	1	0	1	0	0	0	0	–52
:	:	:	:	:	:	:	:	:
1	1	1	1	0	0	0	0	–60
1	1	1	1	0	1	0	0	–66
1	1	1	1	1	0	0	0	–∞
1	1	1	1	1	1	0	0	–∞
:	:	:	:	:	:	:	:	:
1	1	1	1	1	1	1	1	–∞

12.6 Sound feature mode, treble and bass boost settings (write)

Table 34 Register address 12H

BIT	15	14	13	12	11	10	9	8
Symbol	M1	M0	TR1	TR0	BB3	BB2	BB1	BB0
Default	0	0	0	0	0	0	0	0

BIT	7	6	5	4	3	2	1	0
Symbol	–	–	–	–	–	–	–	–
Default	–	–	–	–	–	–	–	–

Table 35 Description of register bits

BIT	SYMBOL	DESCRIPTION
15 to 14	M[1:0]	**Sound feature mode.** A 2-bit value to program the sound processing filter sets (modes) of bass boost and treble. Default value 00, see Table 36.
13 to 12	TR[1:0]	**Treble settings.** A 2-bit value to program the treble setting. The set is selected by the mode bits. Default value 00, see Table 37.
11 to 8	BB[3:0]	**Bass boost settings.** A 4-bit value to program the bass boost settings. The set is selected by the mode bits. Default value 0000, see Table 38.
7 to 0	–	reserved

Table 36 Sound feature mode

M1	M0	MODE SELECTION
0	0	flat set (default)
0	1	minimum set
1	0	
1	1	maximum set

Table 37 Treble settings

TR1	TR0	FLAT SET (dB)	MINIMUM SET (dB)	MAXIMUM SET (dB)
0	0	0	0	0
0	1	0	2	2
1	0	0	4	4
1	1	0	6	6

Table 38 Bass boost settings

BB3	BB2	BB1	BB0	FLAT SET (dB)	MINIMUM SET (dB)	MAXIMUM SET (dB)
0	0	0	0	0	0	0
0	0	0	1	0	2	2
0	0	1	0	0	4	4
0	0	1	1	0	6	6
0	1	0	0	0	8	8
0	1	0	1	0	10	10
0	1	1	0	0	12	12
0	1	1	1	0	14	14
1	0	0	0	0	16	16
1	0	0	1	0	18	18
1	0	1	0	0	18	20
1	0	1	1	0	18	22
1	1	0	0	0	18	24
1	1	0	1	0	18	24
1	1	1	0	0	18	24
1	1	1	1	0	18	24

12.7 De-emphasis and mute (write)

Table 39 Register address 13H

BIT	15	14	13	12	11	10	9	8
Symbol	QMUTE	MT	GS	–	–	DE_2	DE_1	DE_0
Default	0	1	0	–	–	0	0	0

BIT	7	6	5	4	3	2	1	0
Symbol	–	–	–	–	–	–	–	–
Default	–	–	–	–	–	–	–	–

Table 40 Description of register bits

BIT	SYMBOL	DESCRIPTION
15	QMUTE	**Quick mute function.** A 1-bit value to set the quick mute mode. If this bit is logic 0, then the soft mute mode is selected. If this bit is logic 1, then the quick mute mode is selected. Default value 0.
14	MT	**Mute.** A 1-bit value to set the mute function. If this bit is logic 0, then the audio output is not muted (unless pin MUTE is logic 1). If this bit is logic 1, then the audio output is muted. Default value 1.
13	GS	**Gain select.** A 1-bit value to set the gain of the interpolator path. If this bit is logic 0, then the gain is 0 dB. If this bit is logic 1, then the gain is 6 dB. Default value 0.
12 to 11	–	reserved
10 to 8	DE_[2:0]	**De-emphasis select.** A 3-bit value to enable the digital de-emphasis. This setting is only effective in mode 4 to 8. In mode 1 and 3 the information present in the IEC 60958 stream is set automatically. Default value 000, see Table 41.
7 to 0	–	reserved

Table 41 De-emphasis select

DE_2	DE_1	DE_0	FUNCTION
0	0	0	no de-emphasis (default)
0	0	1	32 kHz
0	1	0	44.1 kHz
0	1	1	48 kHz
1	0	0	96 kHz

12.8 DAC source and clock settings (write)

Table 42 Register address 14H

BIT	15	14	13	12	11	10	9	8
Symbol	DA_POL_INV	AUDIO_FS	–	–	–	–	DAC_SEL1	DAC_SEL0
Default	0	1	–	–	–	–	1	0

BIT	7	6	5	4	3	2	1	0
Symbol	–	–	–	–	–	–	–	–
Default	0	–	–	–	–	–	–	–

Table 43 Description of register bits

BIT	SYMBOL	DESCRIPTION
15	DA_POL_INV	**DAC polarity control.** A 1-bit value to control the signal polarity of the DAC output signal. If this bit is logic 0, then the DAC output is not inverted. If this bit is logic 1, then the DAC output is inverted. Default value 0.
14	AUDIO_FS	**Sample frequency range selection.** A 1-bit value to select the sampling frequency range. If this bit is logic 0, then the frequency range is approximately 8 to 50 kHz. The range 8 to 28 kHz is only supported in mode 6 and 7. If this bit is logic 1, then the frequency range is approximately 28 to 100 kHz. Default value 1.
13 to 10	–	reserved
9 to 8	DAC_SEL[1:0]	**DAC input selection.** A 2-bit value to select the data source to the DAC: either the IEC 60958 input or the digital input interface. The DAC clock and the clock input to the FPLL are controlled as well. Default value 10, see Table 44.
7 to 0	–	reserved

Table 44 DAC input selection

DAC_SEL1	DAC_SEL0	DAC INPUT	DAC CLOCK	FPLL INPUT
0	0	input from I^2S-bus	FPLL	SPDIF
0	1	input from I^2S-bus	FPLL	WSI
1	0	input from IEC 60958	FPLL	SPDIF
1	1	input from I^2S-bus	crystal	SPDIF

12.9 SPDIF input settings (write)

Table 45 Register address 30H

BIT	15	14	13	12	11	10	9	8
Symbol	–	–	–	–	–	–	–	–
Default	–	–	–	–	–	–	–	–

BIT	7	6	5	4	3	2	1	0
Symbol	–	–	–	–	COMBINE_ PCM	BURST_ DET_EN	–	SLICE_ SEL
Default	–	–	–	–	1	1	0	0

Table 46 Description of register bits

BIT	SYMBOL	DESCRIPTION
15 to 4	–	reserved
3	COMBINE_PCM	**Combine PCM detection to lock indicator.** A 1-bit value to combine the PCM detection status to the lock indicator. If this bit is logic 0, then the lock indicator does not contain PCM detection status. If this bit is logic 1, then the PCM detection status is combined with the lock indicator. Default value 1.
2	BURST_ DET_EN	**Burst preamble settings.** A 1-bit value to enable auto mute when burst preambles are detected. If this bit is logic 0, then there is no muting. If this bit is logic 1, then there is muting when preambles are detected. Default value 1.
1	–	When writing new settings via the L3-bus or I^2C-bus interface, this bit should always remain at logic 0 (default value) to guarantee correct operation.
0	SLICE_SEL	**Slicer input selection.** A 1-bit value to select an IEC 60958 input signal. If this bit is logic 0, then the input is from pin SPDIF0. If this bit is logic 1, then the input is from pin SPDIF1. Default value 0.

12.10 Supplemental settings (write)

Table 47 Register address 40H

BIT	15	14	13	12	11	10	9	8
Symbol	OSCOUT_EN	–	–	–	–	–	–	–
Default	0	0	0	0	0	0	0	0

BIT	7	6	5	4	3	2	1	0
Symbol	–	–	–	–	–	–	–	–
Default	0	0	0	0	0	0	0	0

Table 48 Description of register bits

BIT	SYMBOL	DESCRIPTION
15	OSCOUT_EN	**Crystal oscillator output control.** A 1-bit value to enable the crystal oscillator output from OSCOUT when PON_XTAL is logic 1. If this bit is logic 0, then no output can be obtained from OSCOUT. If this bit is logic 1 and PON_XTAL is logic 1, then the crystal oscillator output can be obtained from OSCOUT. Default value 0.
14 to 0	–	When writing new settings via the L3-bus or I^2C-bus interface, these bits should always remain at logic 0 (default value) to guarantee correct operation.

12.11 FPLL coarse ratio (write)

Table 49 Register address 62H

BIT	15	14	13	12	11	10	9	8
Symbol	CR15	CR14	CR13	CR12	CR11	CR10	CR9	CR8
Default	0	0	0	0	0	0	1	1

BIT	7	6	5	4	3	2	1	0
Symbol	CR7	CR6	CR5	CR4	CR3	CR2	CR1	CR0
Default	0	0	0	0	0	0	0	0

Table 50 Description of register bits

BIT	SYMBOL	DESCRIPTION
15 to 0	CR[15:0]	**Coarse ratio setting for FPLL.** A 16-bit value to program the coarse ratio for the FPLL in mode 8. Default setting 0300H, see Table 51.

Table 51 Coarse ratio setting for FPLL, note 1

CR15 to CR0	COARSE RATIO
–	$CR15 \times 2^{15} + ... + CR15 \times 2^{0}$

Note

1. In the frequency synthesizer mode (mode 8), combinations of f_i, PR and CR as given in Table 52 are supported. In all other modes, CR[15:0] must be settled to the default value 0300H.

Table 52 Possible combinations of f_i, Pre-scaler Ratio (PR) and Course Ratio (CR)

f_i (kHz)	PR	CR	WS FREQUENCY (kHz)
12000	1/625	320	8000
12000	1/625	441	11025
12000	1/625	882	22050
12000	1/625	1280	32000
12000	1/625	1764	44100
12000	1/625	1920	48000
12288	1/640	320	8000
12288	1/640	441	11025
12288	1/640	882	22050
12288	1/640	1280	32000
12288	1/640	1764	44100
12288	1/640	1920	48000

12.12 Interpolator status (read-out)

Table 53 Register address 18H

BIT	15	14	13	12	11	10	9	8
Symbol	–	–	–	–	–	–	–	–

BIT	7	6	5	4	3	2	1	0
Symbol	–	–	–	–	–	MUTE_ STATE	–	–

Table 54 Description of register bits

BIT	SYMBOL	DESCRIPTION
15 to 3	–	reserved
2	MUTE_STATE	**Mute status bit.** A 1-bit value to indicate the status of the mute function. If this bit is logic 0, then the audio output is not muted. If this bit is logic 1, then the mute sequence has been completed and the audio output is muted.
1 to 0	–	reserved

12.13 SPDIF status (read-out)

Table 55 Register address 59H

BIT	15	14	13	12	11	10	9	8
Symbol	–	–	–	–	–	–	–	–

BIT	7	6	5	4	3	2	1	0
Symbol	–	–	–	–	SLICE_ STAT	BURST_ DET	B_ERR	SPDIFIN_ LOCK

Table 56 Description of register bits

BIT	SYMBOL	DESCRIPTION
15 to 4	–	reserved
3	SLICE_STAT	**Slicer source status.** A 1-bit value to indicate which SPDIF input pin is selected as the input source. If this bit is logic 0, then the IEC 60958 input is from pin SPDIF0. If this bit is logic 1, then the IEC 60958 input is from pin SPDIF1.
2	BURST_DET	**Burst preamble detection.** A 1-bit value to signal whether burst preamble words are detected in the SPDIF stream or not. If this bit is logic 0, then no preamble words are detected. If this bit is logic 1, then burst-payload is detected.
1	B_ERR	**Bit error detection.** A 1-bit value to signal whether there are bit errors detected in the SPDIF stream or not. If this bit is logic 0, then no errors are detected. If this bit is logic 1, then bi-phase errors are detected.
0	SPDIFIN_LOCK	**SPDIF lock indicator.** A 1-bit value to signal whether the SPDIF decoder block is in lock or not. If this bit is logic 0, then the decoder block is out-of-lock. If this bit is logic 1, then the decoder block is in lock.

12.14 Channel status (read-out)

12.14.1 CHANNEL STATUS BITS LEFT [15:0]

Table 57 Register address 5AH

BIT	15	14	13	12	11	10	9	8
Symbol	SPDI_ BIT15	SPDI_ BIT14	SPDI_ BIT13	SPDI_ BIT12	SPDI_ BIT11	SPDI_ BIT10	SPDI_ BIT9	SPDI_ BIT8

BIT	7	6	5	4	3	2	1	0
Symbol	SPDI_ BIT7	SPDI_ BIT6	SPDI_ BIT5	SPDI_ BIT4	SPDI_ BIT3	SPDI_ BIT2	SPDI_ BIT1	SPDI_ BIT0

12.14.2 CHANNEL STATUS BITS LEFT [31:16]

Table 58 Register address 5BH

BIT	15	14	13	12	11	10	9	8
Symbol	SPDI_ BIT31	SPDI_ BIT30	SPDI_ BIT29	SPDI_ BIT28	SPDI_ BIT27	SPDI_ BIT26	SPDI_ BIT25	SPDI_ BIT24

BIT	7	6	5	4	3	2	1	0
Symbol	SPDI_ BIT23	SPDI_ BIT22	SPDI_ BIT21	SPDI_ BIT20	SPDI_ BIT19	SPDI_ BIT18	SPDI_ BIT17	SPDI_ BIT16

12.14.3 CHANNEL STATUS BITS LEFT [39:32]

Table 59 Register address 5CH

BIT	15	14	13	12	11	10	9	8
Symbol	–	–	–	–	–	–	–	–

BIT	7	6	5	4	3	2	1	0
Symbol	SPDI_ BIT39	SPDI_ BIT38	SPDI_ BIT37	SPDI_ BIT36	SPDI_ BIT35	SPDI_ BIT34	SPDI_ BIT33	SPDI_ BIT32

12.14.4 CHANNEL STATUS BITS RIGHT [15:0]

Table 60 Register address 5DH

BIT	15	14	13	12	11	10	9	8
Symbol	SPDI_ BIT15	SPDI_ BIT14	SPDI_ BIT13	SPDI_ BIT12	SPDI_ BIT11	SPDI_ BIT10	SPDI_ BIT9	SPDI_ BIT8

BIT	7	6	5	4	3	2	1	0
Symbol	SPDI_ BIT7	SPDI_ BIT6	SPDI_ BIT5	SPDI_ BIT4	SPDI_ BIT3	SPDI_ BIT2	SPDI_ BIT1	SPDI_ BIT0

12.14.5 CHANNEL STATUS BITS RIGHT [31:16]

Table 61 Register address 5EH

BIT	15	14	13	12	11	10	9	8
Symbol	SPDI_ BIT31	SPDI_ BIT30	SPDI_ BIT29	SPDI_ BIT28	SPDI_ BIT27	SPDI_ BIT26	SPDI_ BIT25	SPDI_ BIT24

BIT	7	6	5	4	3	2	1	0
Symbol	SPDI_ BIT23	SPDI_ BIT22	SPDI_ BIT21	SPDI_ BIT20	SPDI_ BIT19	SPDI_ BIT18	SPDI_ BIT17	SPDI_ BIT16

12.14.6 CHANNEL STATUS BITS RIGHT [39:32]

Table 62 Register address 5FH

BIT	15	14	13	12	11	10	9	8
Symbol	–	–	–	–	–	–	–	–

BIT	7	6	5	4	3	2	1	0
Symbol	SPDI_ BIT39	SPDI_ BIT38	SPDI_ BIT37	SPDI_ BIT36	SPDI_ BIT35	SPDI_ BIT34	SPDI_ BIT33	SPDI_ BIT32

Table 63 Description of register bits (two times 40 bits indicating the left and right channel status)

BIT	SYMBOL	DESCRIPTION
39 to 36	–	reserved but undefined at present
35 to 33	SPDI_BIT[35:33]	**Word length.** A 3-bit value indicating the word length. See Table 64.
32	SPDI_BIT[32]	**Audio sample word length.** A 1-bit value to signal the maximum audio sample word length. If bit 32 is logic 0, then the maximum length is 20 bits. If bit 32 is logic 1, then the maximum length is 24 bits.
31 to 30	SPDI_BIT[31:30]	reserved
29 to 28	SPDI_BIT[29:28]	**Clock accuracy.** A 2-bit value indicating the clock accuracy. See Table 65.
27 to 24	SPDI_BIT[27:24]	**Sample frequency.** A 4-bit value indicating the sampling frequency. See Table 66.
23 to 20	SPDI_BIT[23:20]	**Channel number.** A 4-bit value indicating the channel number. See Table 67.
19 to 16	SPDI_BIT[19:16]	**Source number.** A 4-bit value indicating the source number. See Table 68.
15 to 8	SPDI_BIT[15:8]	**General information.** A 8-bit value indicating general information. See Table 69.
7 to 6	SPDI_BIT[7:6]	**Mode.** A 2-bit value indicating mode 0. See Table 70.
5 to 3	SPDI_BIT[5:3]	**Audio sampling.** A 3-bit value indicating the type of audio sampling. See Table 71.
2	SPDI_BIT2	**Software copyright.** A 1-bit value indicating software for which copyright is asserted or not. If this bit is logic 0, then copyright is asserted. If this bit is logic 1, then no copyright is asserted.
1	SPDI_BIT1	**Audio sample word.** A 1-bit value indicating the type of audio sample word. If this bit is logic 0, then the audio sample word represents linear PCM samples. If this bit is logic 1, then the audio sample word is used for other purposes.
0	SPDI_BIT0	**Channel status.** A 1-bit value indicating the consumer use of the status block. This bit is logic 0.

Table 64 Word length

SPDI_BIT35	SPDI_BIT34	SPDI_BIT33	WORD LENGTH	
			SPDI_BIT32 = 0	SPDI_BIT32 = 1
0	0	0	word length not indicated (default)	word length not indicated (default)
0	0	1	16 bits	20 bits
0	1	0	18 bits	22 bits
0	1	1	reserved	reserved
1	0	0	19 bits	23 bits
1	0	1	20 bits	24 bits
1	1	0	17 bits	21 bits
1	1	1	reserved	reserved

Table 65 Clock accuracy

SPDI_BIT29	SPDI_BIT28	CLOCK ACCURACY
0	0	level II
0	1	level I
1	0	level III
1	1	reserved

Table 66 Sampling frequency

SPDI_BIT27	SPDI_BIT26	SPDI_BIT25	SPDI_BIT24	SAMPLING FREQUENCY
0	0	0	0	44.1 kHz
0	0	0	1	48 kHz
0	0	1	0	32 kHz
:	:	:	:	other states reserved
1	1	1	1	

Table 67 Channel number

SPDI_BIT23	SPDI_BIT22	SPDI_BIT21	SPDI_BIT20	CHANNEL NUMBER
0	0	0	0	don’t care
0	0	0	1	A (left for stereo transmission)
0	0	1	0	B (right for stereo transmission)
0	0	1	1	C
0	1	0	0	D
0	1	0	1	E
0	1	1	0	F
0	1	1	1	G
1	0	0	0	H
1	0	0	1	I
1	0	1	0	J
1	0	1	1	K

SPDI_BIT23	SPDI_BIT22	SPDI_BIT21	SPDI_BIT20	CHANNEL NUMBER
1	1	0	0	L
1	1	0	1	M
1	1	1	0	N
1	1	1	1	O

Table 68 Source number

SPDI_BIT19	SPDI_BIT18	SPDI_BIT17	SPDI_BIT16	SOURCE NUMBER
0	0	0	0	don’t care
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8
1	0	0	1	9
1	0	1	0	10
1	0	1	1	11
1	1	0	0	12
1	1	0	1	13
1	1	1	0	14
1	1	1	1	15

Table 69 General information

SPDI_BIT[15:8]	FUNCTION
000 00000	general
100 xxxxL	laser optical products
010 xxxxL	digital-to-digital converters and signal processing products
110 xxxxL	magnetic tape or disc based products
001 xxxxL	broadcast reception of digitally encoded audio signals with video signals
011 1xxxL	broadcast reception of digitally encoded audio signals without video signals
101 xxxxL	musical instruments, microphones and other sources without copyright information
011 00xxL	analog-to-digital converters for analog signals without copyright information
011 01xxL	analog-to-digital converters for analog signals which include copyright information in the form of ‘Cp- and L-bit status’
000 1xxxL	solid state memory based products
000 0001L	experimental products not for commercial sale
111 xxxxL	reserved
000 0xxxL	reserved, except 000 0000 and 000 0001L

Table 70 Mode

SPDI_BIT7	SPDI_BIT6	MODE
0	0	mode 0
0	1	reserved
1	0	
1	1	

Table 71 Audio sampling

SPDI_BIT5	SPDI_BIT4	SPDI_BIT3	AUDIO SAMPLE	
			SPDI_BIT1 = 0	SPDI_BIT1 = 1
0	0	0	2 audio samples without pre-emphasis	default state for applications other than linear PCM
0	0	1	2 audio samples with 50/15 μs pre-emphasis	other states reserved
0	1	0	reserved (2 audio samples with pre-emphasis)	
0	1	1	reserved (2 audio samples with pre-emphasis)	
:	:	:	other states reserved	
1	1	1		

12.15 FPLL status (read-out)

Table 72 Register address 68H

BIT	15	14	13	12	11	10	9	8
Symbol	–	–	–	–	–	–	–	FPLL_ LOCK

BIT	7	6	5	4	3	2	1	0
Symbol	–	–	–	VCO_ TIMEOUT	–	–	–	–

Table 73 Description of register bits

BIT	SYMBOL	DESCRIPTION
15 to 9	–	reserved
8	FPLL_LOCK	**FPLL lock.** A 1-bit value that indicates the FPLL status together with bit 4, see Table 74.
7 to 5	–	reserved
4	VCO_TIMEOUT	**VCO time-out.** A 1-bit value that indicates the FPLL status together with bit 8, see Table 74.
3 to 0	–	reserved

Table 74 Lock status indicators of the FPLL

FPLL_LOCK	VCO_TIMEOUT	FUNCTION
0	0	FPLL out-of-lock
0	1	FPLL time-out
1	0	FPLL in lock
1	1	FPLL time-out

12.16 Device information (read-out)

Table 75 Register address 7EH

BIT	15	14	13	12	11	10	9	8
Symbol	TP11	TP10	TP9	TP8	TP7	TP6	TP5	TP4
Default	0	1	0	1	0	1	0	0

BIT	7	6	5	4	3	2	1	0
Symbol	TP3	TP2	TP1	TP0	VER3	VER2	VER1	VER0
Default	1	0	0	0	0	0	1	1

Table 76 Description of register bits

BIT	SYMBOL	DESCRIPTION
15 to 4	TP[11:0]	**Device type.** A 12-bit value to indicate the device type information. Read-out value is always fixed.
3 to 0	VER[3:0]	**Device version.** A 4-bit value to indicate the device version information. Read-out value is always fixed.

13 LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DD}	supply voltage	note 1	2.4	5.0	V
T_{xtal}	crystal temperature		–25	+150	°C
T_{stg}	storage temperature		–65	+125	°C
T_{amb}	ambient temperature		–40	+85	°C
V_{esd}	electrostatic discharge voltage	Human Body Model (HBM); note 2	–2000	+2000	V
		Machine Model (MM); note 3	–200	+200	V
$I_{lu(prot)}$	latch-up protection current	T_{amb} = 125 °C; V_{DD} = 3.6 V	–	200	mA
$I_{sc(DAC)}$	short-circuit current of DAC	T_{amb} = 0 °C; V_{DD} = 3 V; note 4			
		output short-circuited to $V_{SSA(DAC)}$	–	20	mA
		output short-circuited to $V_{DDA(DAC)}$	–	100	mA

Notes

1. All V_{DD} and V_{SS} connections must be made to the same power supply.
2. JEDEC class 2 compliant.
3. JEDEC class B compliant, except pin $V_{SSA(PLL)}$, which can withstand ESD pulses of –130 to +130 V.
4. DAC operation after short-circuiting cannot be warranted.

14 THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	85	K/W

15 CHARACTERISTICS

$V_{DDD} = V_{DDA} = 3.0$ V; IEC 60958 input with $f_s = 48.0$ kHz; $T_{amb} = 25$ °C; $R_L = 5$ kΩ; all voltages measured with respect to ground; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies; note 1						
V_{DDA}	analog supply voltage		2.4	3.0	3.6	V
$V_{DDA(DAC)}$	analog supply voltage for DAC		2.4	3.0	3.6	V
$V_{DDA(PLL)}$	analog supply voltage for PLL		2.4	3.0	3.6	V
V_{DDD}	digital supply voltage		2.4	3.0	3.6	V
$V_{DDD(C)}$	digital supply voltage for core		2.4	3.0	3.6	V
$I_{DDA(DAC)}$	analog supply current of DAC	power-on	–	3.3	–	mA
		power-down; clock off	–	35	–	μA
$I_{DDA(PLL)}$	analog supply current of PLL	at 48 kHz	–	0.5	–	mA
		at 96 kHz	–	0.7	–	mA
$I_{DDD(C)}$	digital supply current of core	at 48 kHz	–	9	–	mA
		at 96 kHz	–	17	–	mA
I_{DDD}	digital supply current	at 48 kHz	–	0.6	–	mA
		at 96 kHz	–	1.2	–	mA
P_{48}	power consumption at 48 kHz	DAC in Playback mode	–	40	–	mW
		DAC in Power-down mode	–	tbf	–	mW
P_{96}	power consumption at 96 kHz	DAC in Playback mode	–	67	–	mW
		DAC in Power-down mode	–	tbf	–	mW
Digital inputs						
V_{IH}	HIGH-level input voltage		$0.8V_{DDD}$	–	$V_{DDD} + 0.5$	V
V_{IL}	LOW-level input voltage		–0.5	–	$+0.2V_{DDD}$	V
$\lvert I_{LI} \rvert$	input leakage current		–	–	10	μA
C_i	input capacitance		–	–	10	pF
$R_{pu(int)}$	internal pull-up resistance		16	33	78	kΩ
$R_{pd(int)}$	internal pull-down resistance		16	33	78	kΩ
Digital outputs						
V_{OH}	HIGH-level output voltage	$I_{OH} = -2$ mA	$0.85V_{DDD}$	–	–	V
V_{OL}	LOW-level output voltage	$I_{OL} = 2$ mA	–	–	0.4	V
$I_{O(max)}$	maximum output current		–	3	–	mA
Digital-to-analog converter; note 2						
$V_{o(rms)}$	output voltage (RMS value)	$f_i = 1.0$ kHz tone at 0 dBFS; note 3	850	900	950	mV
ΔV_o	unbalance of output voltages	$f_i = 1.0$ kHz tone	–	0.1	0.4	dB
V_{ref}	reference voltage	measured with respect to V_{SSA}	$0.45V_{DDA}$	$0.50V_{DDA}$	$0.55V_{DDA}$	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
(THD+N)/S	total harmonic distortion-plus-noise to signal ratio	f_i = 1.0 kHz tone at 48 kHz				
		at 0 dBFS	–	–90	–83	dB
		at –40 dBFS; A-weighted	–	–60	–52	dB
		f_i = 1.0 kHz tone at 96 kHz				
		at 0 dBFS	–	–85	–78	dB
		at –40 dBFS; A-weighted	–	–57	–52	dB
S/N_{48}	signal-to-noise ratio at 48 kHz	f_i = 1.0 kHz tone; code = 0; A-weighted	95	100	–	dB
S/N_{96}	signal-to-noise ratio at 96 kHz	f_i = 1.0 kHz tone; code = 0; A-weighted	92	97	–	dB
α_{cs}	channel separation	f_i = 1.0 kHz tone	–	110	–	dB
SPDIF inputs						
$V_{i(p-p)}$	AC input voltage (peak-to-peak value)		0.2	0.5	3.3	V
R_i	input resistance		–	6	–	kΩ
V_{hys}	hysteresis voltage		–	40	–	mV

Notes

1. All supply pins V_{DD} and V_{SS} must be connected to the same external power supply unit.
2. When the DAC must drive a higher capacitive load (above 50 pF), a series resistor of 100 Ω must be used to prevent oscillations in the output stage of the operational amplifier.
3. The output voltage of the DAC is proportional to the DAC power supply voltage.

16 TIMING CHARACTERISTICS

V_{DDD} = V_{DDA} = 2.4 to 3.6 V; T_{amb} = −40 to +85 °C; R_L = 5 kΩ; all voltages measured with respect to ground; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	UNIT
Device reset					
t_{rst}	reset active time		–	250	µs
PLL lock time					
t_{lock}	time-to-lock	f_s = 32.0 kHz	–	85.0	ms
		f_s = 44.1 kHz	–	63.0	ms
		f_s = 48.0 kHz	–	60.0	ms
		f_s = 96.0 kHz	–	40.0	ms
L3-bus microcontroller interface (see Figs 17 and 18)					
$T_{cy(CLK)(L3)}$	L3CLOCK cycle time		500	–	ns
$t_{CLK(L3)H}$	L3CLOCK HIGH time		250	–	ns
$t_{CLK(L3)L}$	L3CLOCK LOW time		250	–	ns
$t_{su(L3)A}$	L3MODE set-up time in address mode		190	–	ns
$t_{h(L3)A}$	L3MODE hold time in address mode		190	–	ns
$t_{su(L3)D}$	L3MODE set-up time in data transfer mode		190	–	ns
$t_{h(L3)D}$	L3MODE hold time in data transfer mode		190	–	ns
$t_{(stp)(L3)}$	L3MODE stop time in data transfer mode		190	–	ns
$t_{su(L3)DA}$	L3DATA set-up time in address and data transfer mode		190	–	ns
$t_{h(L3)DA}$	L3DATA hold time in address and data transfer mode		30	–	ns
$t_{su(L3)R}$	L3DATA set-up time in data transfer mode	read mode	50	–	ns
$t_{h(L3)R}$	L3DATA hold time in data transfer mode	read mode	360	–	ns

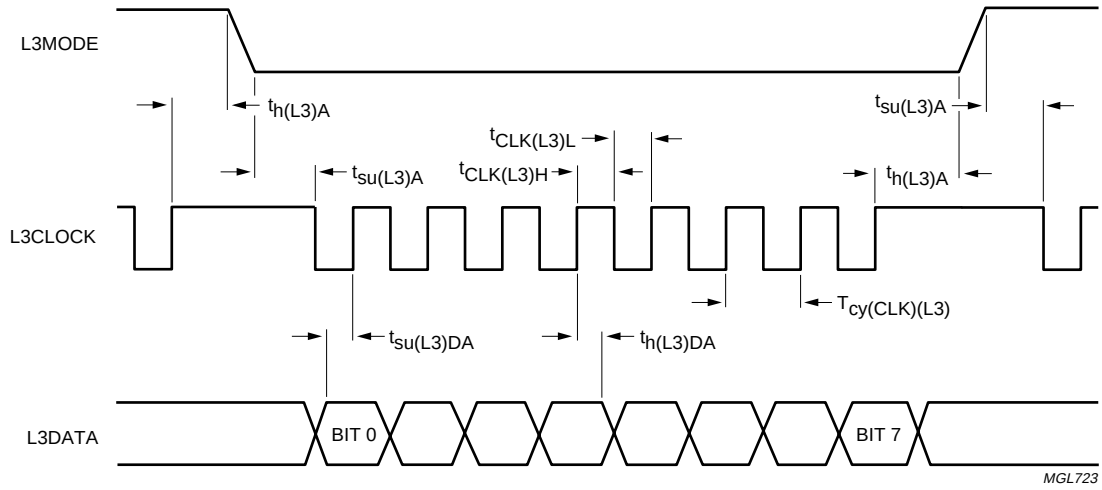


Fig.17 Timing for address mode.

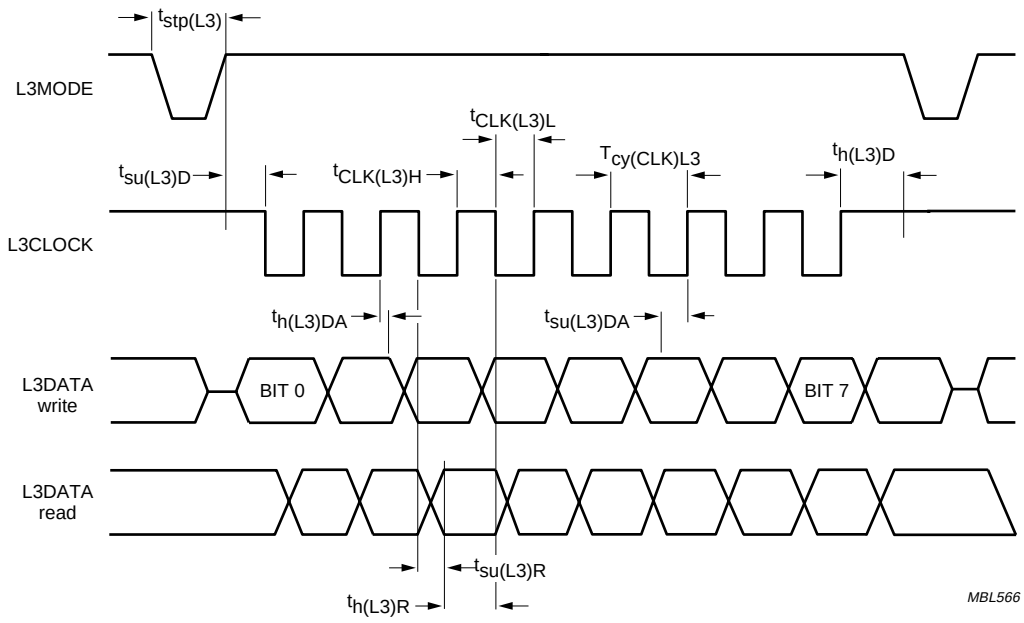


Fig.18 Timing for data transfer mode.

17 APPLICATION INFORMATION

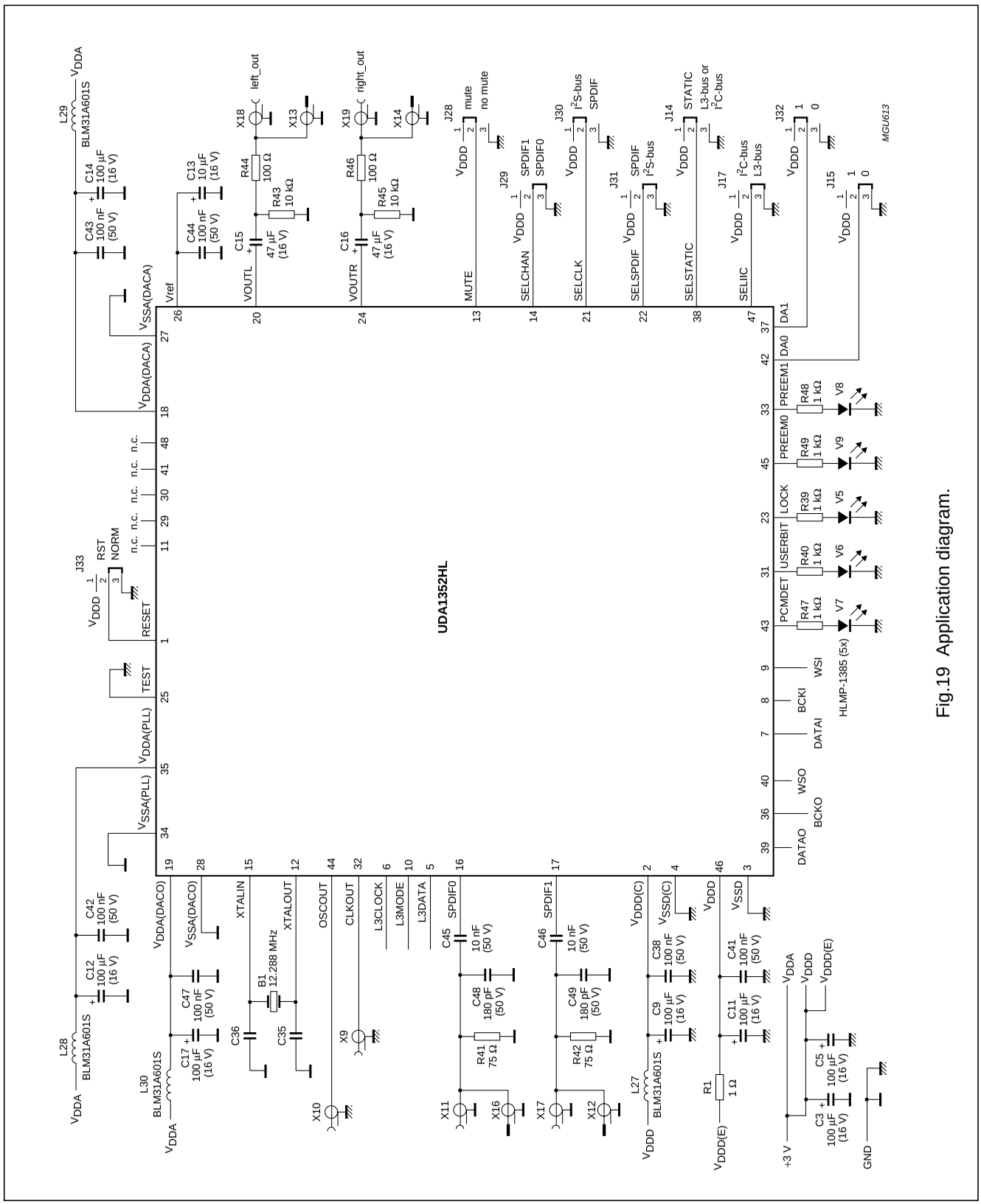
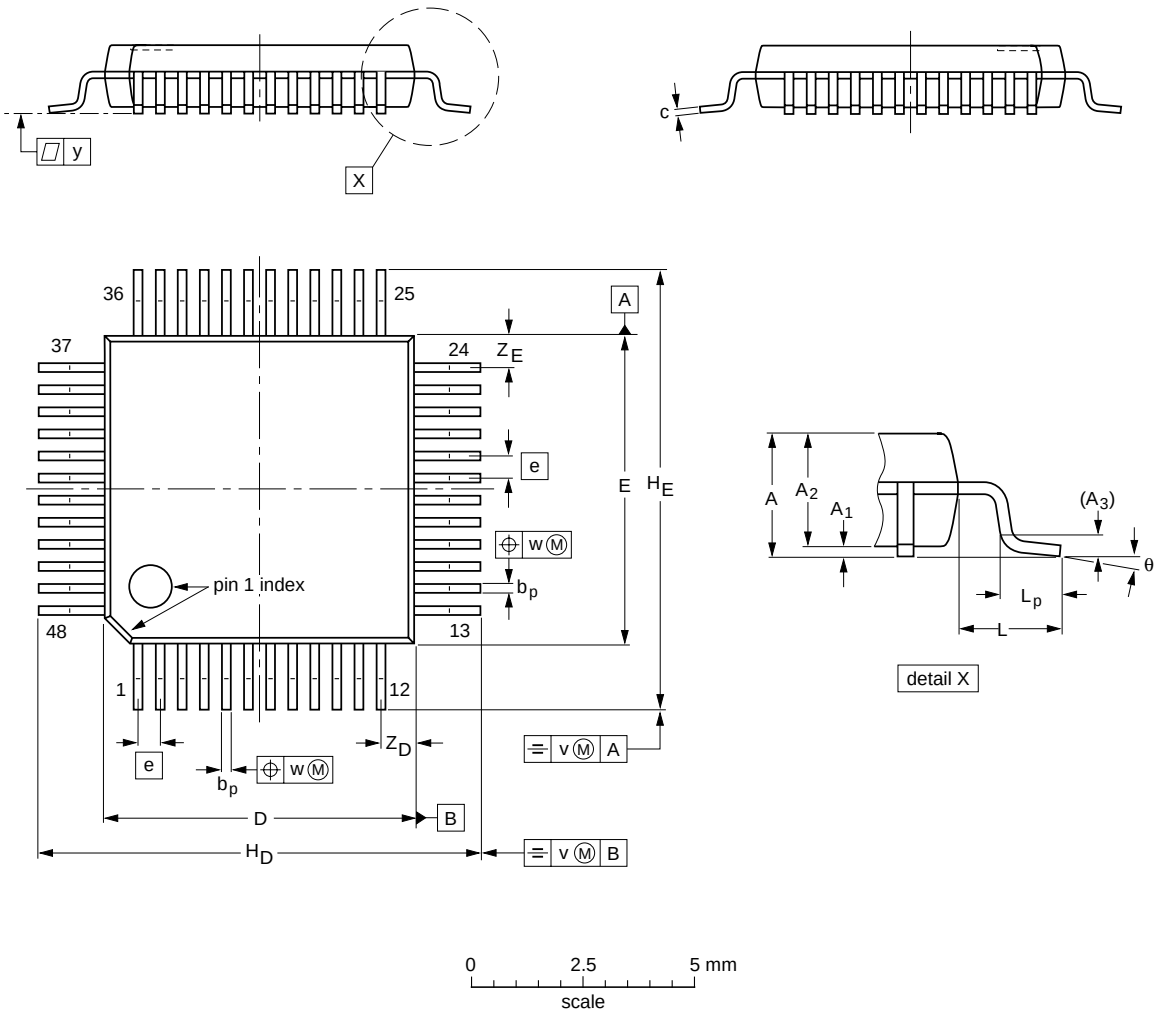


Fig.19 Application diagram.

18 PACKAGE OUTLINE

LQFP48: plastic low profile quad flat package; 48 leads; body 7 x 7 x 1.4 mm **SOT313-2**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	1.60	0.20 0.05	1.45 1.35	0.25	0.27 0.17	0.18 0.12	7.1 6.9	7.1 6.9	0.5	9.15 8.85	9.15 8.85	1.0	0.75 0.45	0.2	0.12	0.1	0.95 0.55	0.95 0.55	7^o 0^o

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT313-2	136E05	MS-026				~~99-12-27~~ 00-01-19

19 SOLDERING

19.1 Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering can still be used for certain surface mount ICs, but it is not suitable for fine pitch SMDs. In these situations reflow soldering is recommended.

19.2 Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, convection or convection/infrared heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 250 °C. The top-surface temperature of the packages should preferable be kept below 220 °C for thick/large packages, and below 235 °C for small/thin packages.

19.3 Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

  The footprint must incorporate solder thieves at the downstream end.
- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time is 4 seconds at 250 °C.
A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

19.4 Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

19.5 Suitability of surface mount IC packages for wave and reflow soldering methods

PACKAGE[1]	SOLDERING METHOD	
	WAVE	REFLOW[2]
BGA, LBGA, LFBGA, SQFP, TFBGA, VFBGA	not suitable	suitable
HBCC, HBGA, HLQFP, HSQFP, HSOP, HTQFP, HTSSOP, HVQFN, HVSON, SMS	not suitable[3]	suitable
PLCC[4], SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended[4][5]	suitable
SSOP, TSSOP, VSO	not recommended[6]	suitable

Notes

1. For more detailed information on the BGA packages refer to the *"(LF)BGA Application Note*" (AN01026); order a copy from your Philips Semiconductors sales office.
2. All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *"Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods"*.
3. These packages are not suitable for wave soldering. On versions with the heatsink on the bottom side, the solder cannot penetrate between the printed-circuit board and the heatsink. On versions with the heatsink on the top side, the solder might be deposited on the heatsink surface.
4. If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
5. Wave soldering is suitable for LQFP, TQFP and QFP packages with a pitch (e) larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
6. Wave soldering is suitable for SSOP and TSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

20 DATA SHEET STATUS

DATA SHEET STATUS[1]	PRODUCT STATUS[2]	DEFINITIONS
Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Changes will be communicated according to the Customer Product/Process Change Notification (CPCN) procedure SNW-SQ-650A.

Notes

1. Please consult the most recently issued data sheet before initiating or completing a design.
2. The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.

21 DEFINITIONS

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Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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23 PURCHASE OF PHILIPS I²C COMPONENTS

Purchase of Philips I²C components conveys a license under the Philips' I²C patent to use the components in the I²C system provided the system conforms to the I²C specification defined by Philips. This specification can be ordered using the code 9398 393 40011.

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Contact information

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